

AMD AM4.

GAMING EDGE AC

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MS-7C37

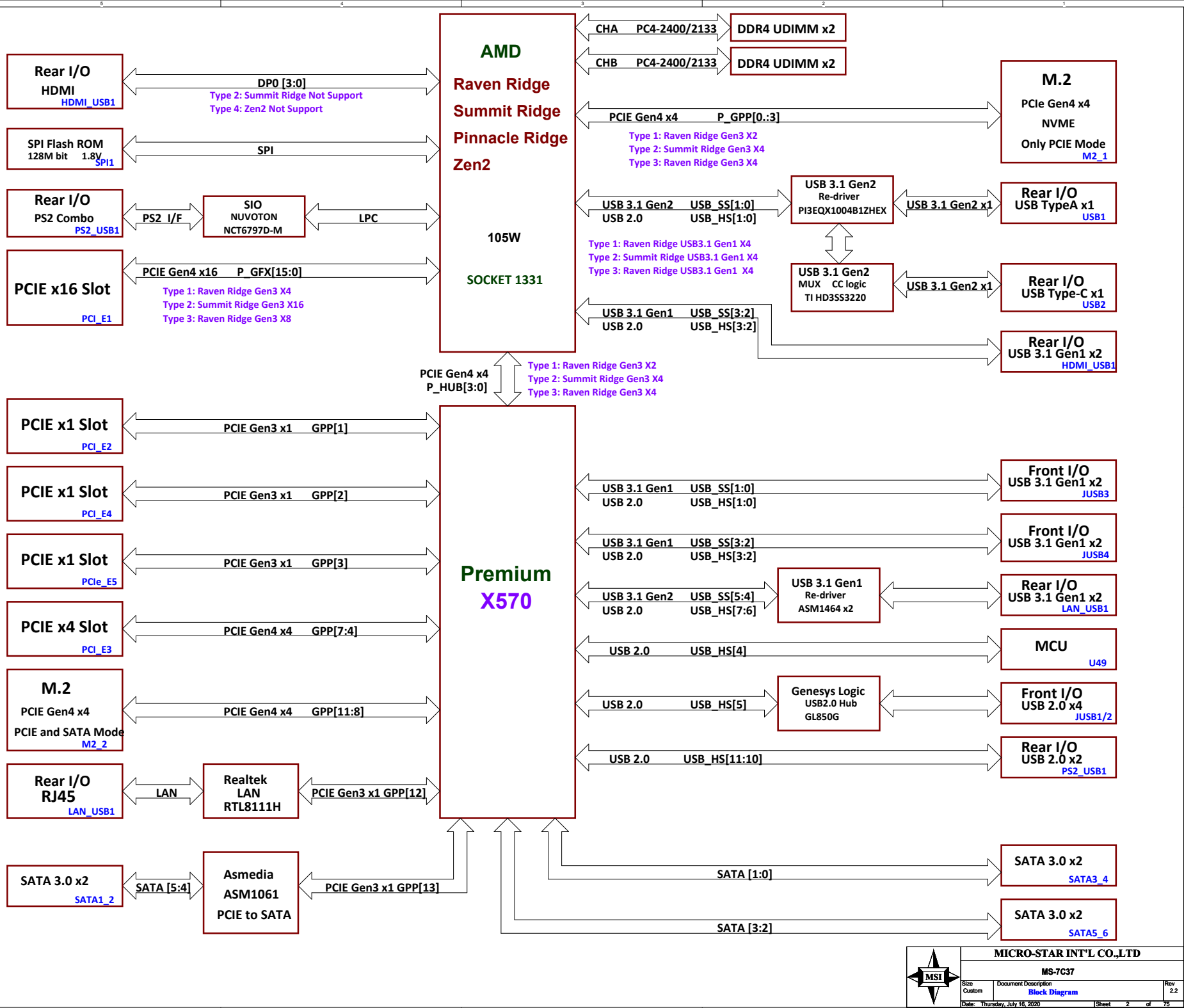
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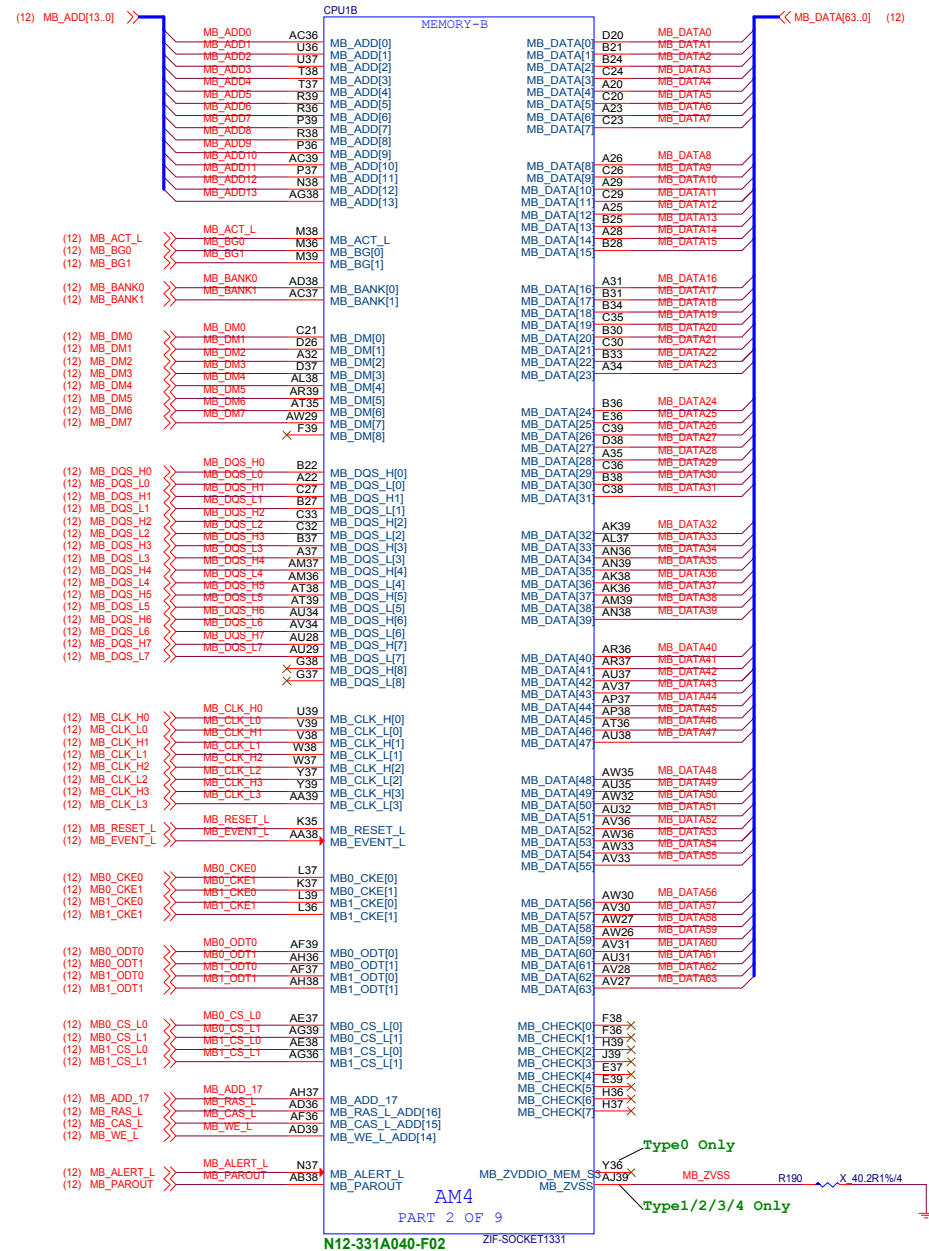
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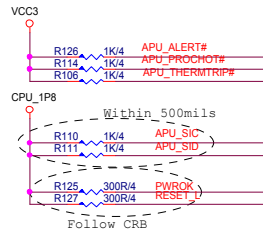
Rev
2.2

Date: Thursday, July 16, 2020

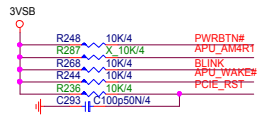
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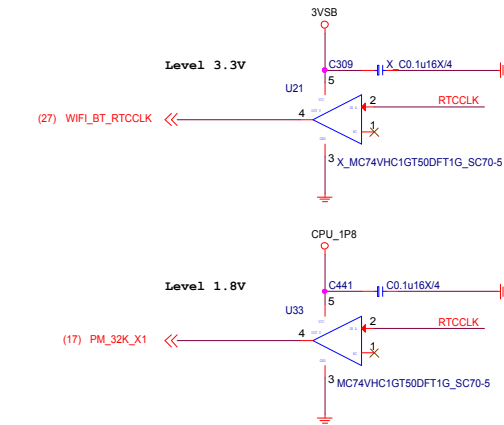
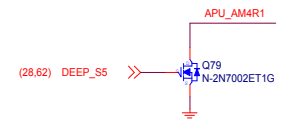




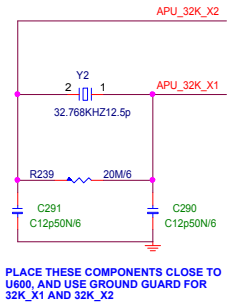
Add for HDT and close to PIN E16 & B16



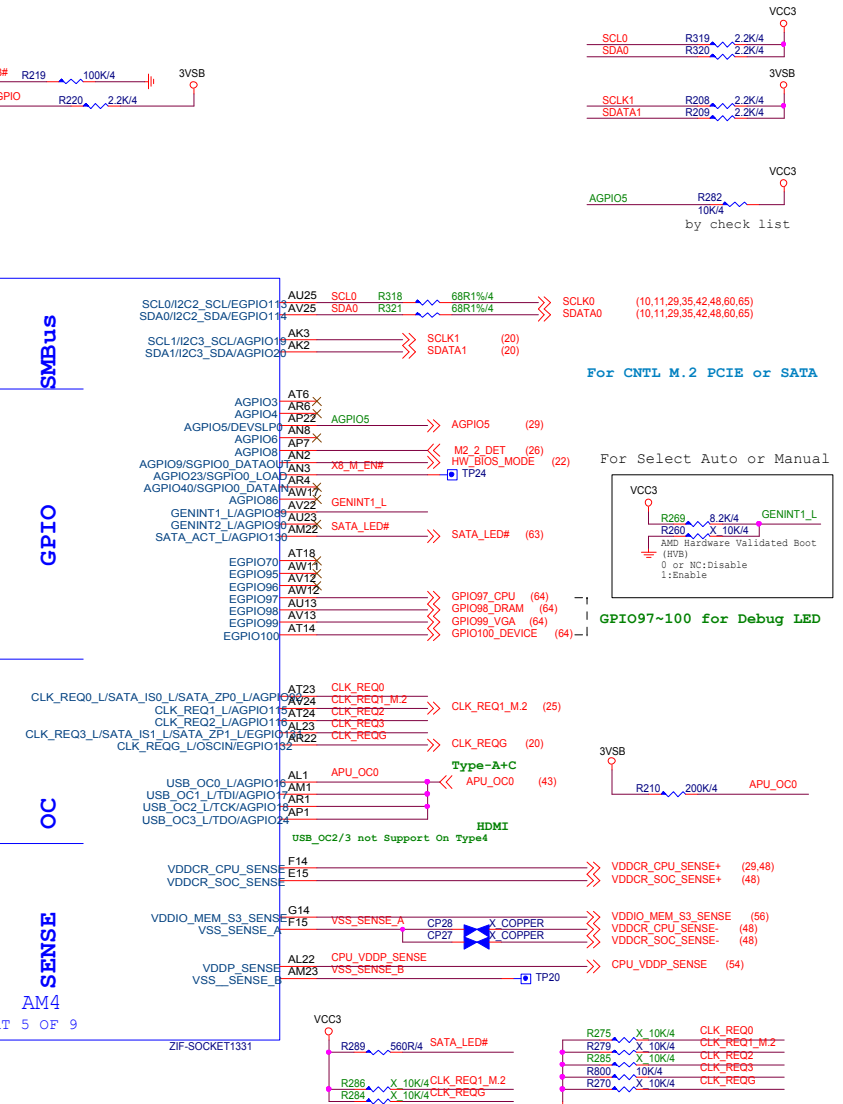
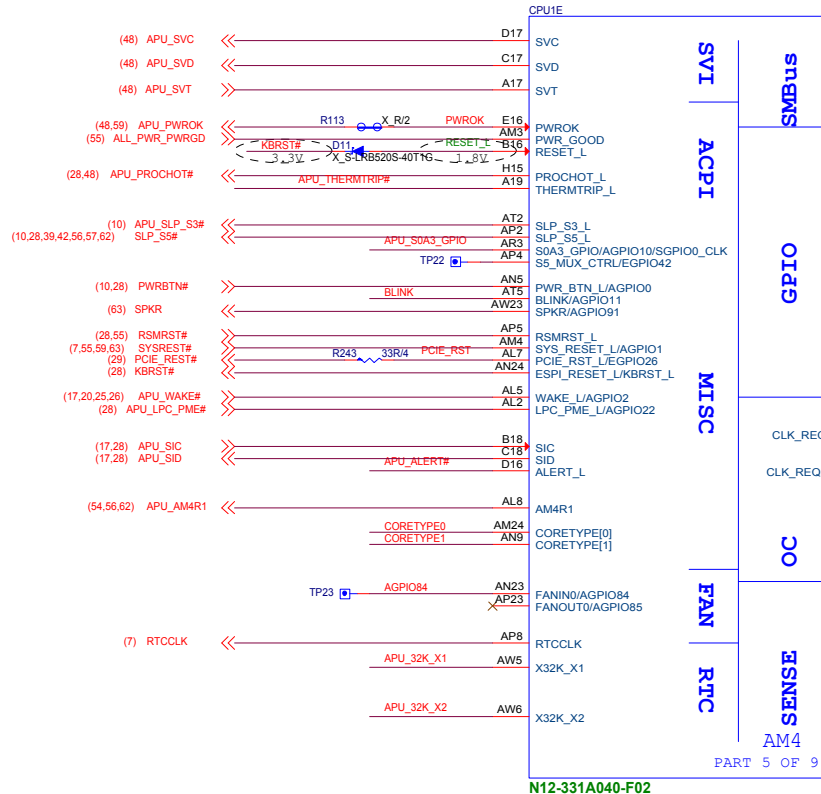
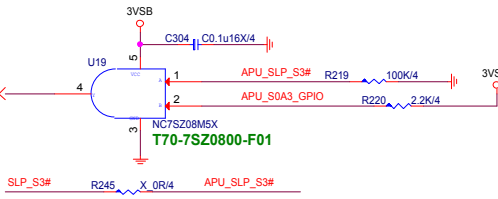
Turn off power when BIOS into deep mode



Layout: Place x'tal within 1.5 inch of APU



AM4 CPU TYPE Circuit



$$I_B = (CPU_1P8_S5 - V_{be}) / 5.7k$$

$$(1.8 - 0.95) / 5.7k = 0.149mA$$

$$I_C = (VCC5 - V_{ce}) / 47k$$

$$(5 - 0.2) / 47k = 0.102mA$$

TYPE0_CPU_SEL
0: RV
1: BR/SR/PR/MTS

TYPE0_CPU_SEL (7,54,55)

SPEC no Support

CPU	TYPE	CORETYPE1	CORETYPE0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	1



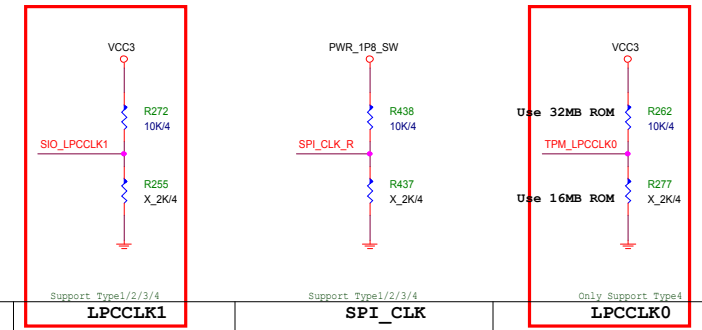
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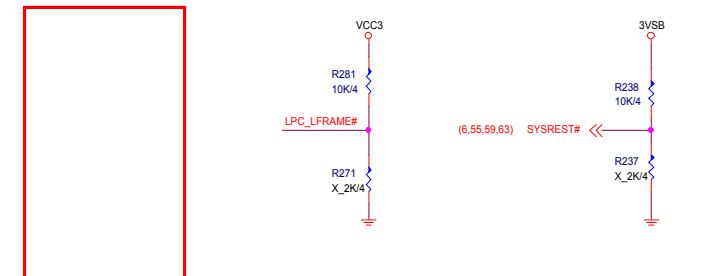
Size	Document Description	Rev
Custom	AM4 SVI/ACPI/GPIO	2.2

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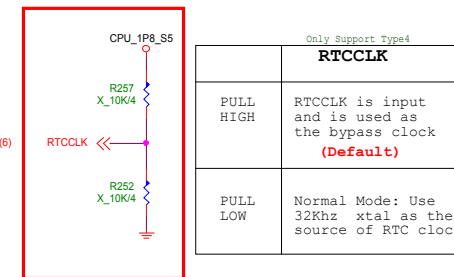
Strapping Options



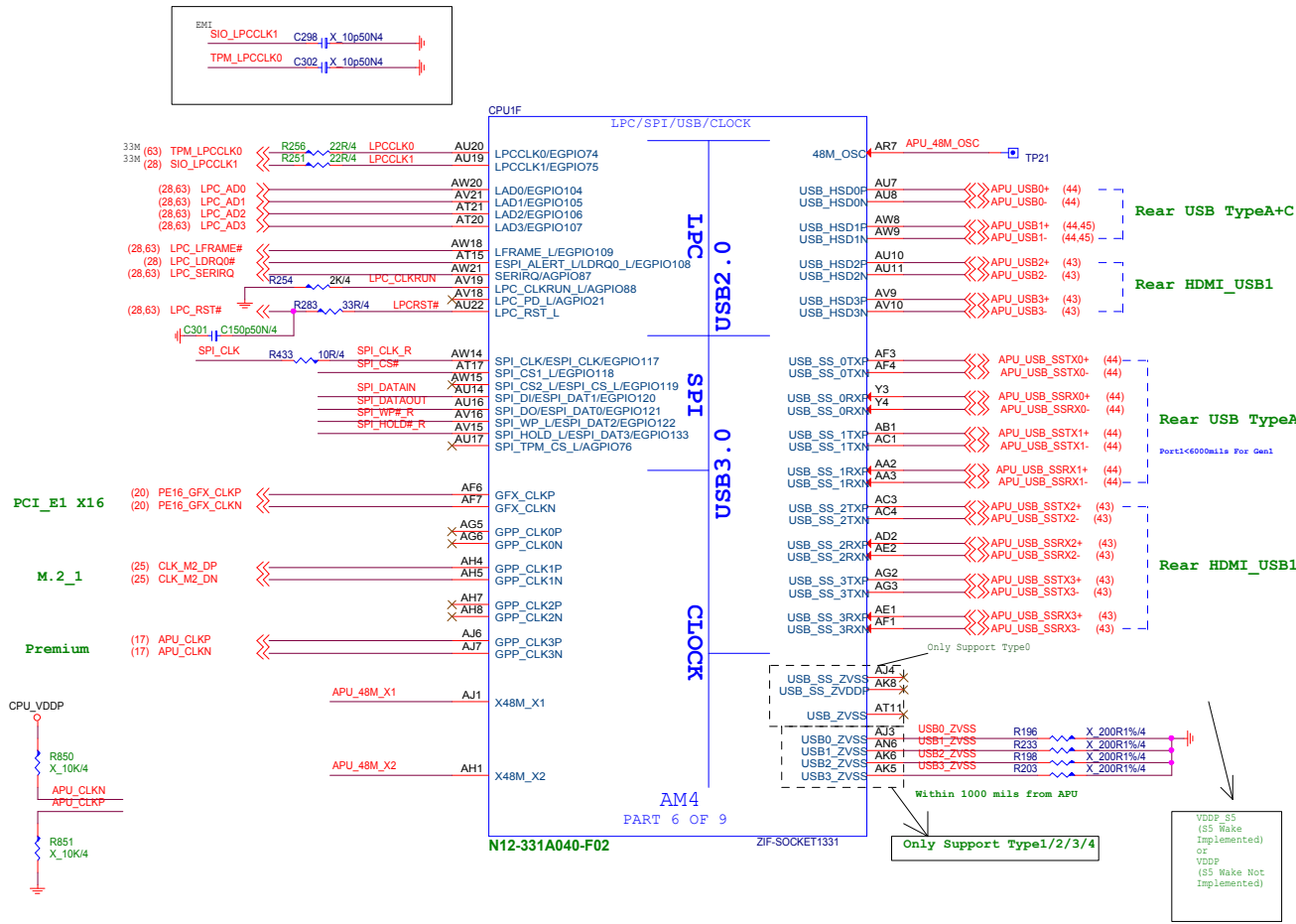
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]



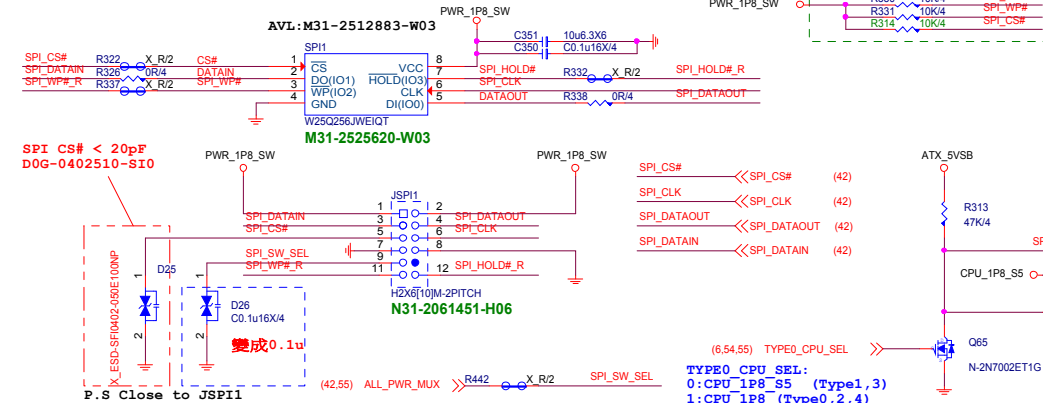
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode



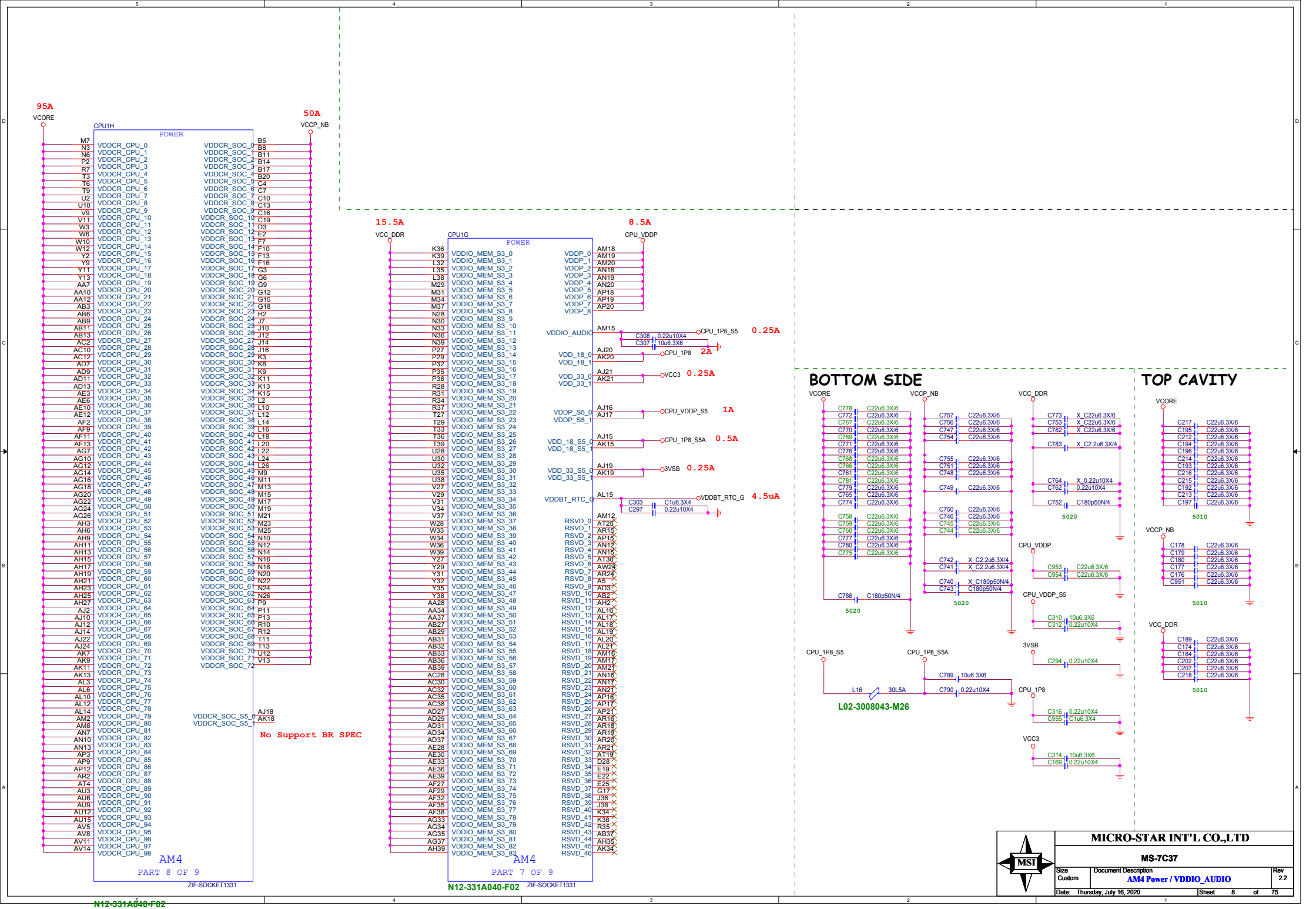
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 2.2
AM4 LPC / SPI / USB / CLK / STRAP		
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SPI ROM(1.8V)



TYPE0 CPU SEL:
0: CPU_1P8_S5 (Type1, 3)
1: CPU_1P8 (Type0, 2, 4)



GND

AM4
PART 9 OF 9

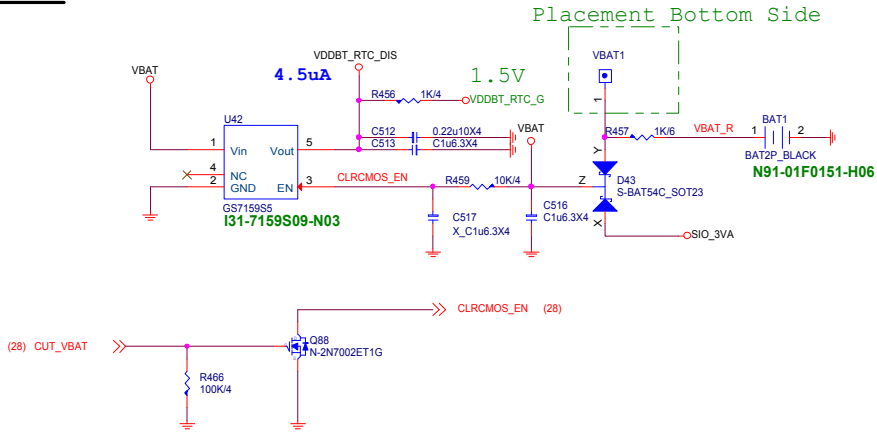


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Size	Document Description	Rev
Custom	AM4 GND	2.2
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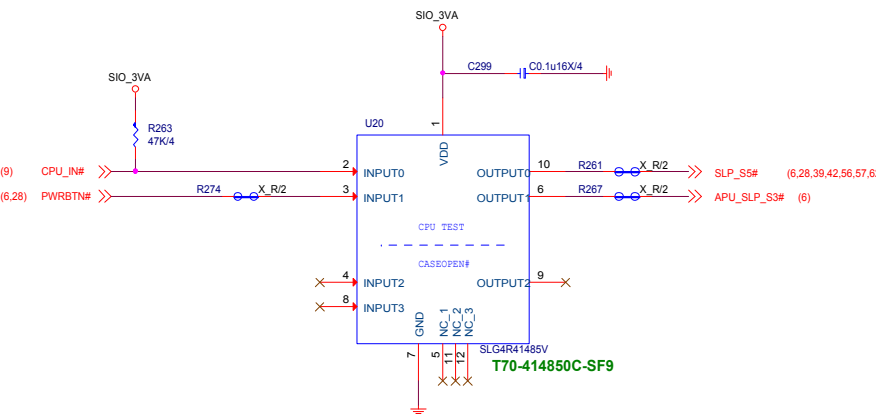
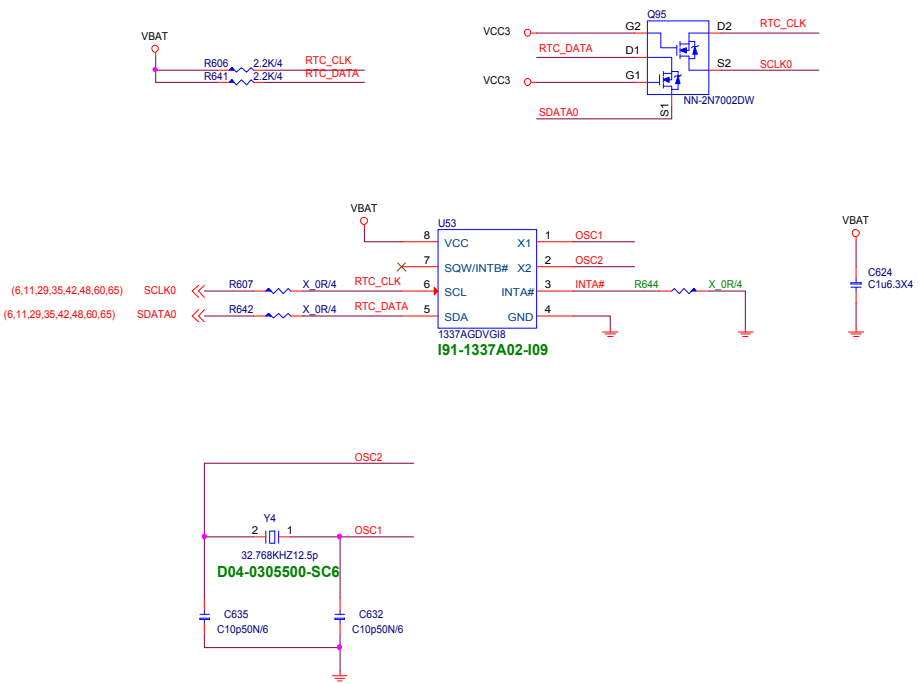
RTC & Clear CMOS Circuit



Clear CMOS button

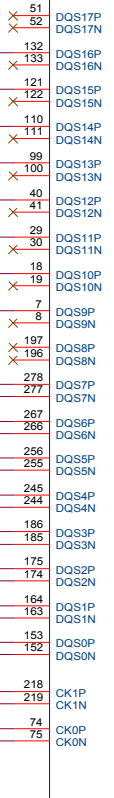


RTC Backup

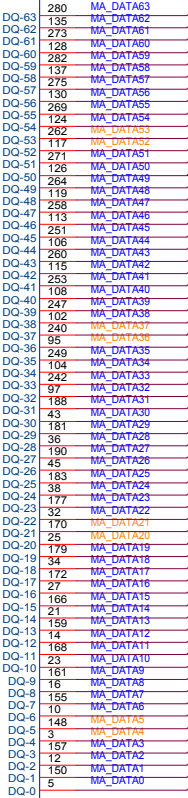


A1 A2 B1 B2

DIMMA1A



DDRIV-288P_BLACK
N13-2880551-L06



<< MA_DATA[63..0] (3)

56-63

48-55

40-47

32-39

24-31

16-23

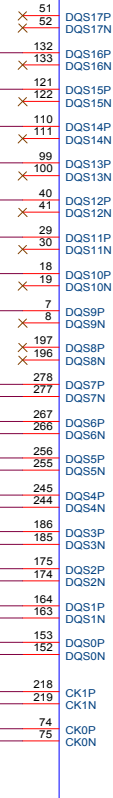
8-15

0-7

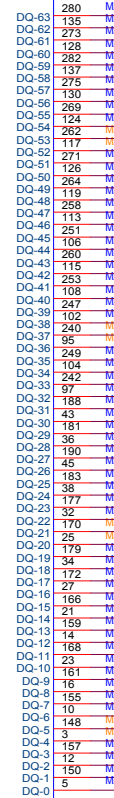
SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMB1	A6



DIMMA2A



DIMMA2A



<< MA_DATA[63..0] (3)

56-63

48-55

40-47

32-39

24-31

16-23

8-15

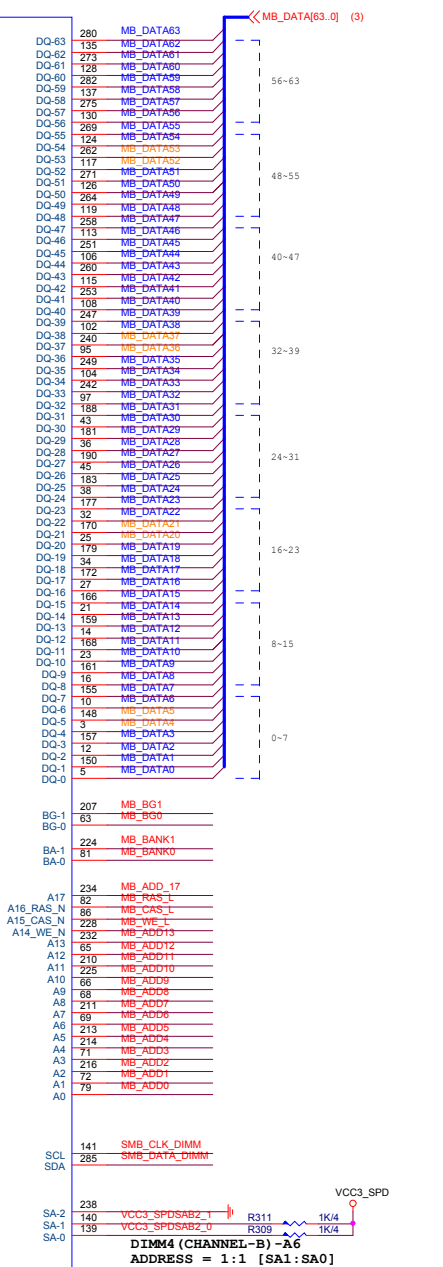
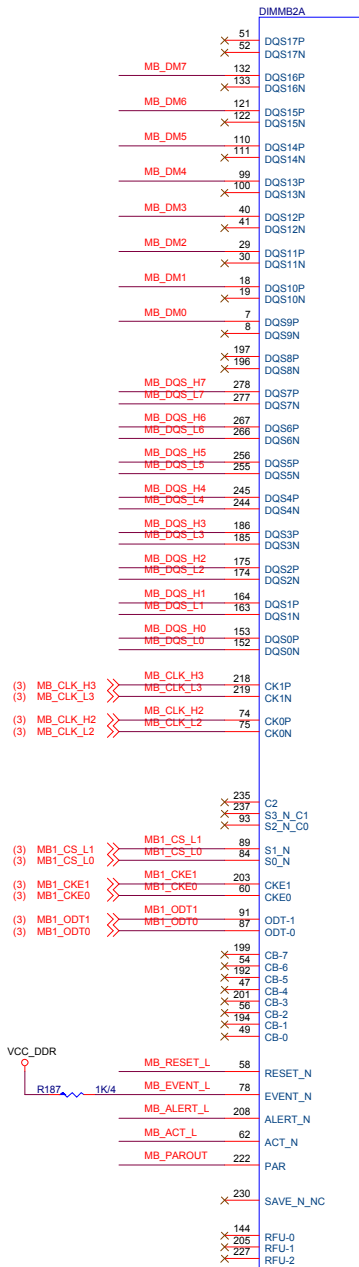
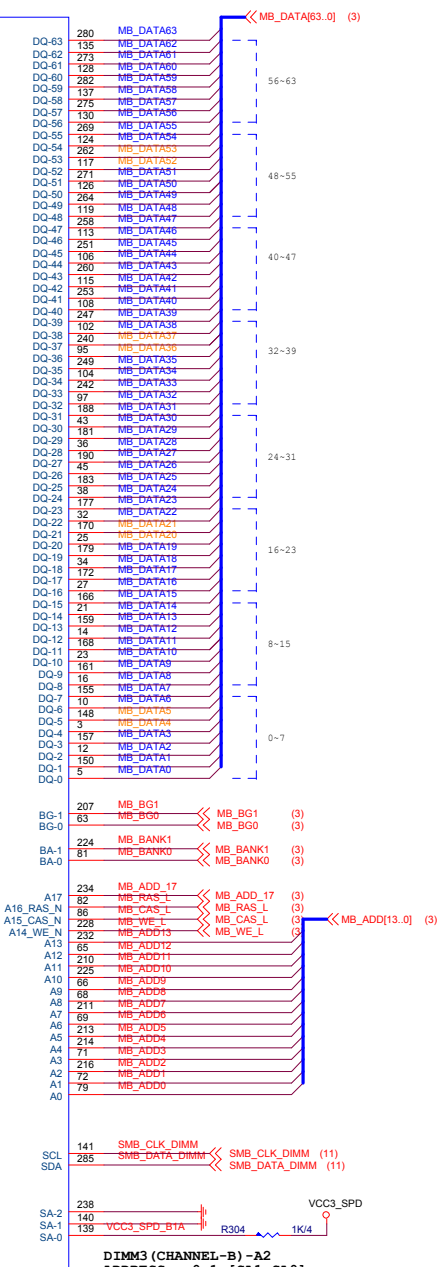
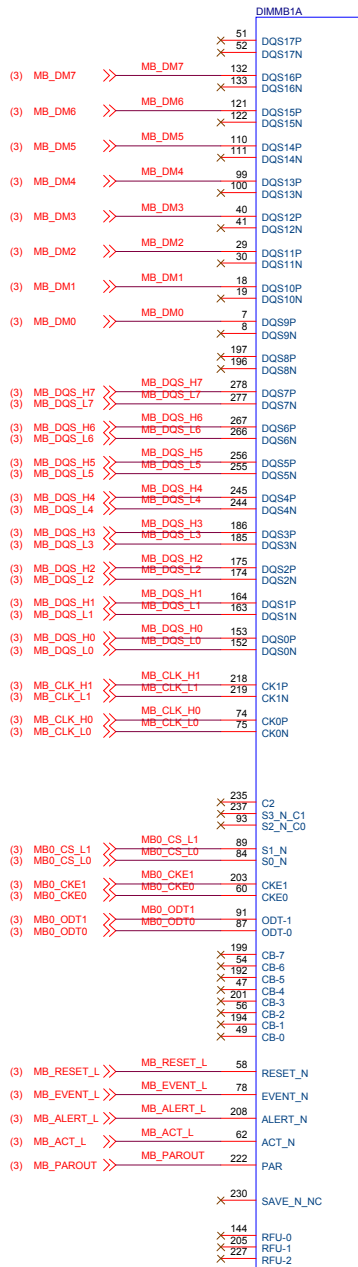
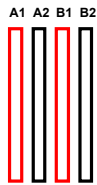
0-7

DDRIV-288P_BLACK
N13-2880551-L06



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MS-7C37			
Size	Document Description	Rev	
Custom	DDR4 - DIMM CH-A	2.2	
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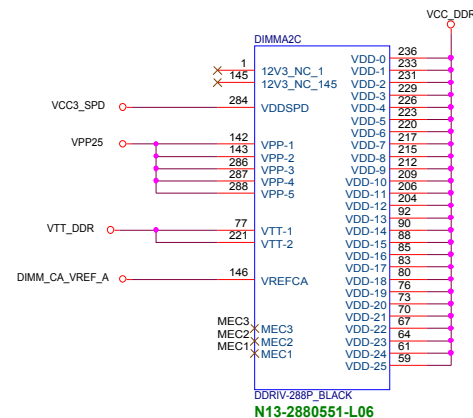
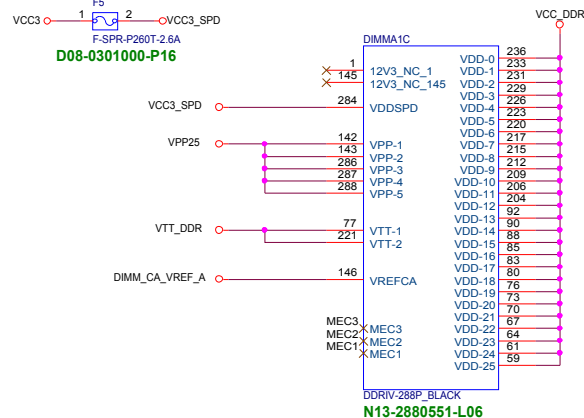
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size	Document Description	Rev
Custom	DDR4 - DIMM CH-B	2.2
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av1:D08-0301100-B07

VCC3 1 F5 2 VCC3_SPD
F-SPR-P280T-2.6A

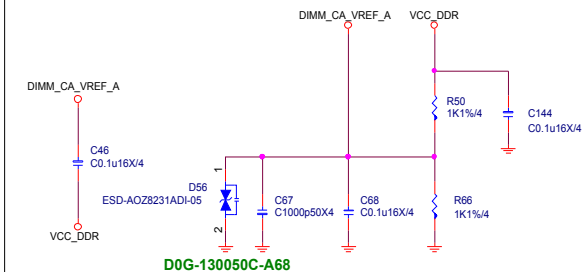
D08-0301000-P16

DIMM SLOT PN BY SPEC

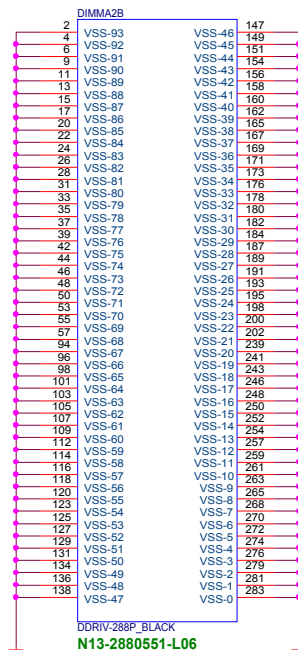
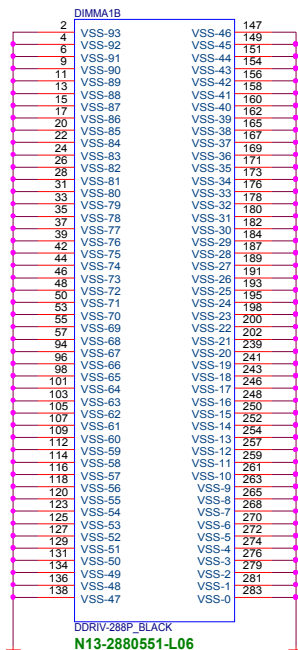
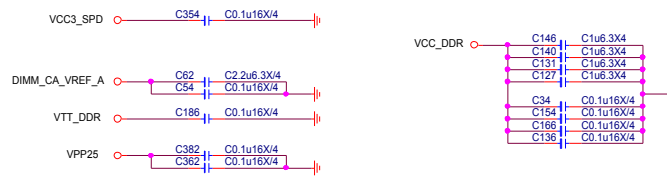
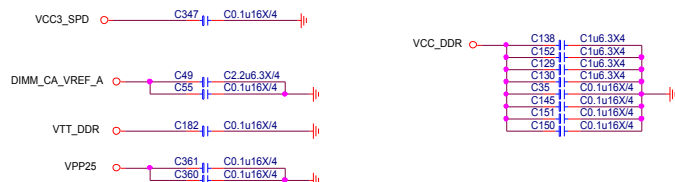


DDR VREF

(place resistors close to DIMMs)



D0G-130050C-A68



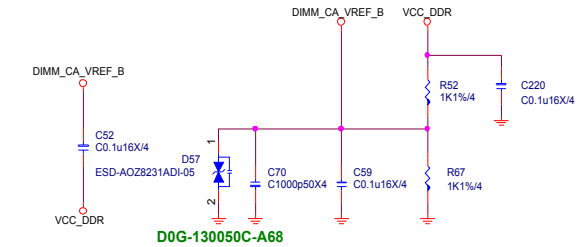
MICRO-STAR INT'L CO.,LTD

MS-7C37

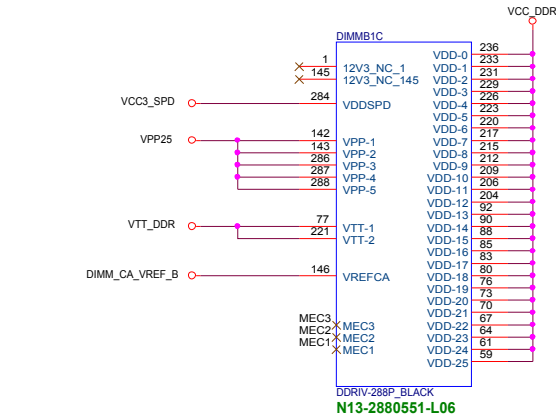
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DDR VREF

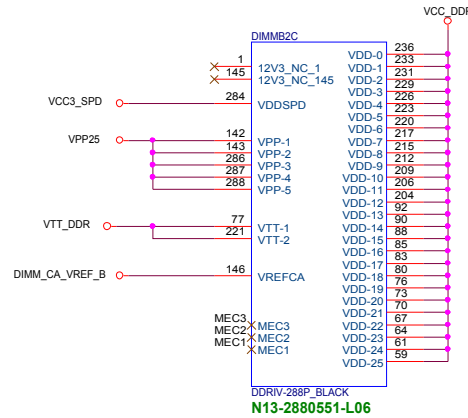
(place resistors close to DIMMs)



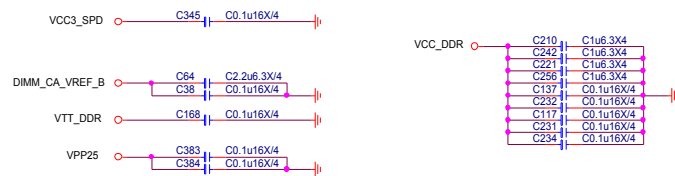
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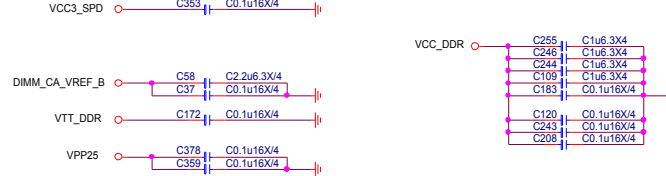
DDRIV-288P_BLACK
N13-2880551-L06



DDRIV-288P_BLACK
N13-2880551-L06



DDRIV-288P_BLACK
N13-2880551-L06



DDRIV-288P_BLACK
N13-2880551-L06

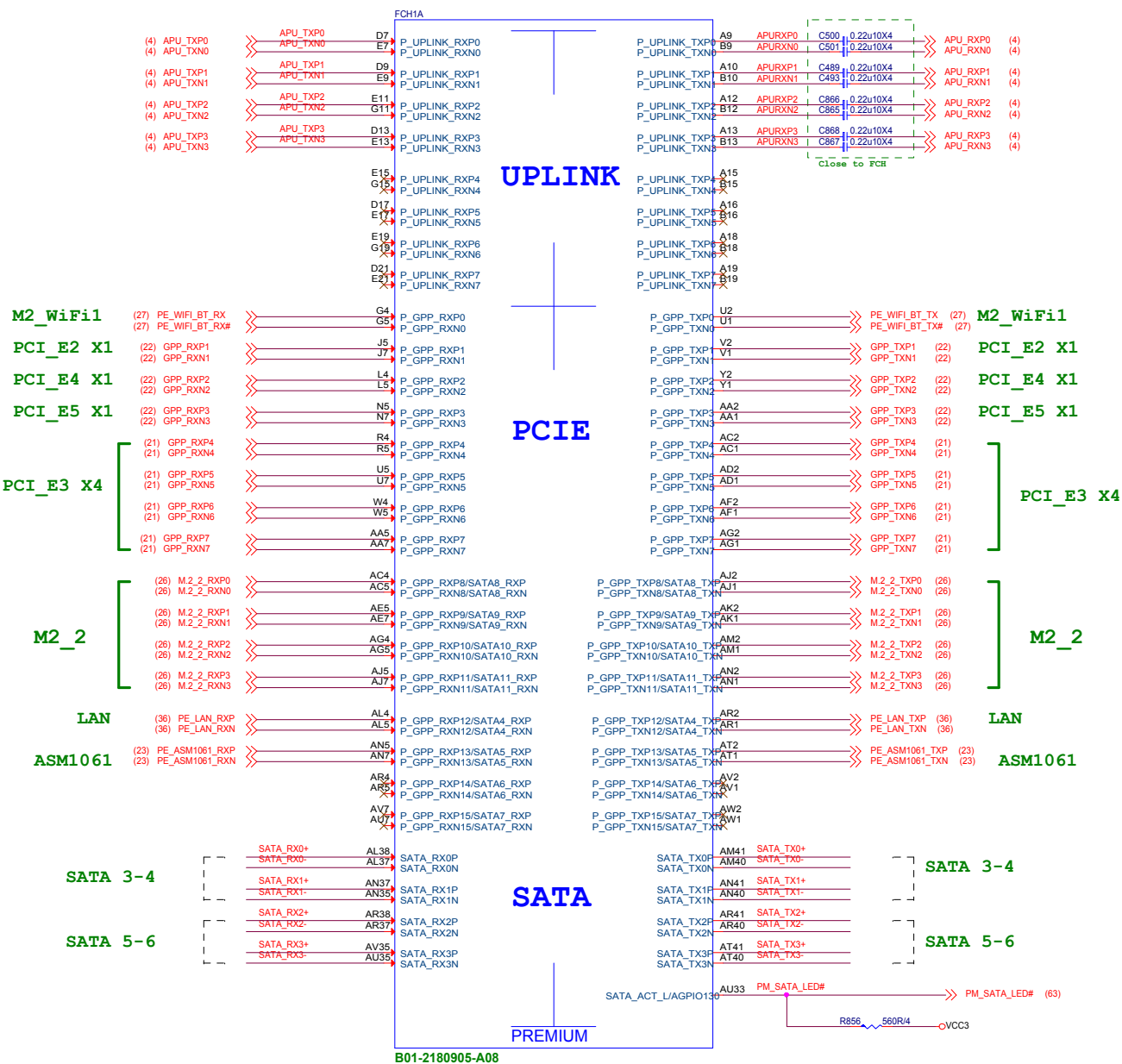
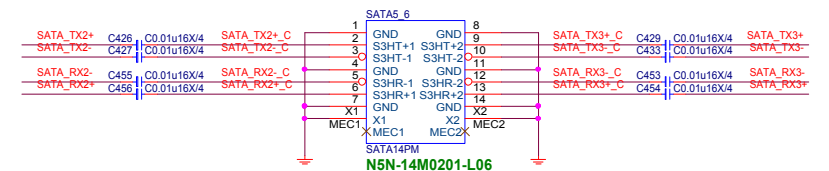
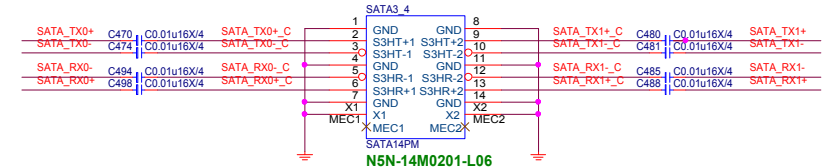


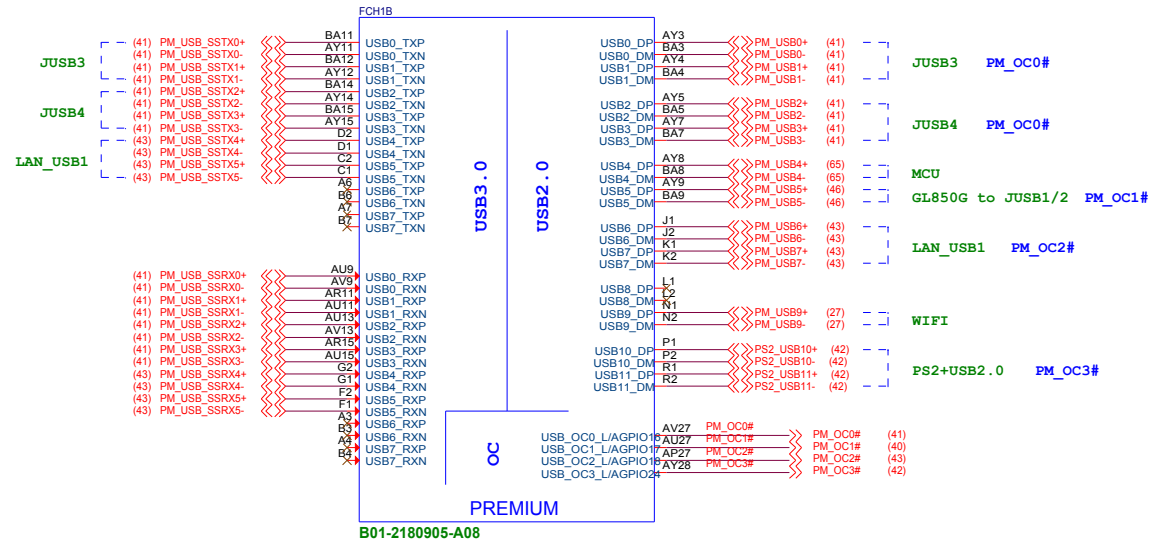
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Size	Document Description	Rev
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Date:	Thursday, July 16, 2020	Sheet 14 of 75

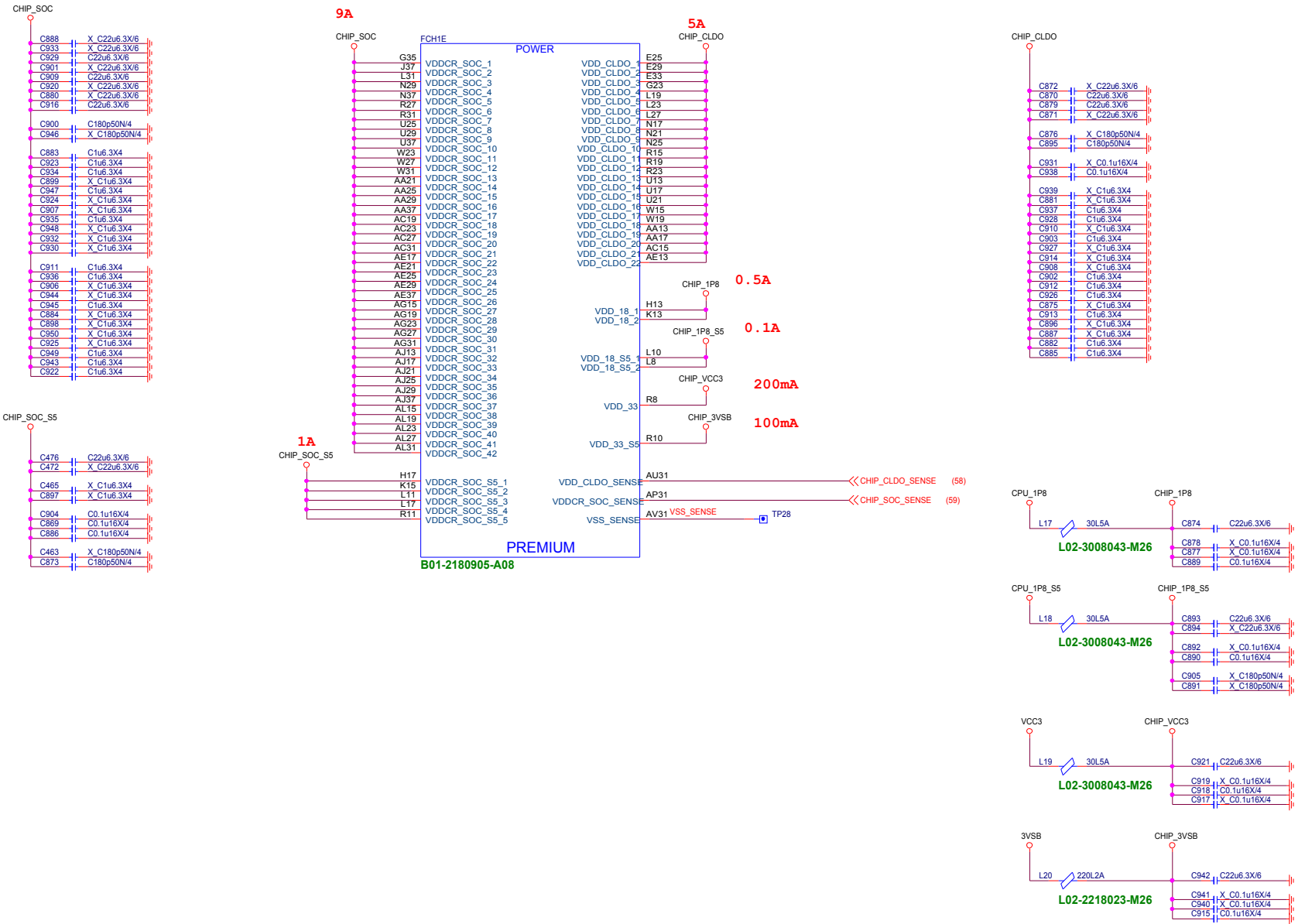
SATA Connector

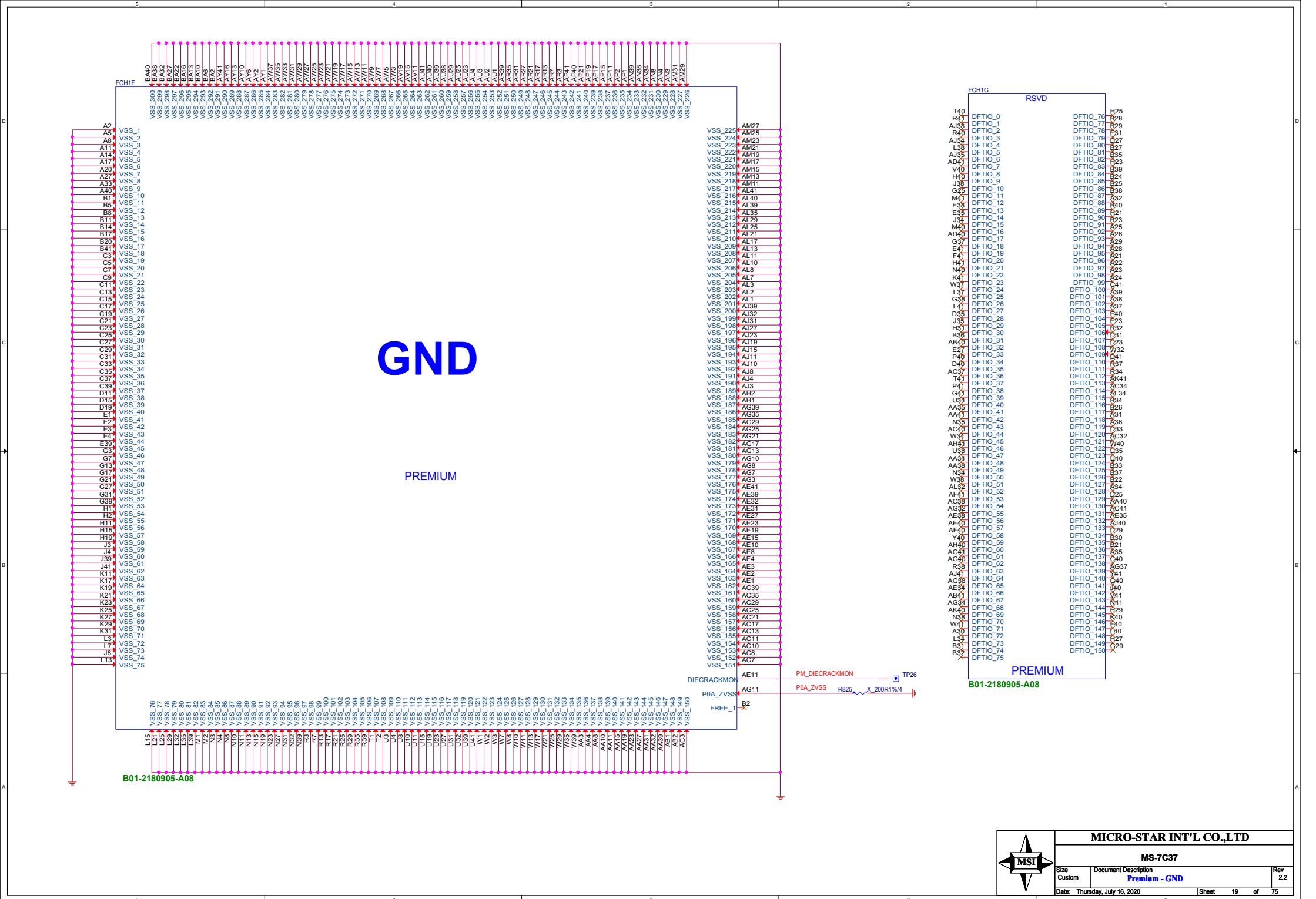




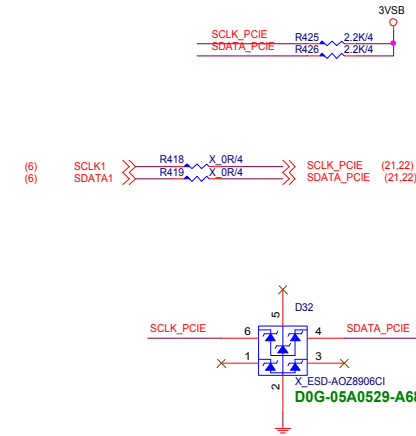
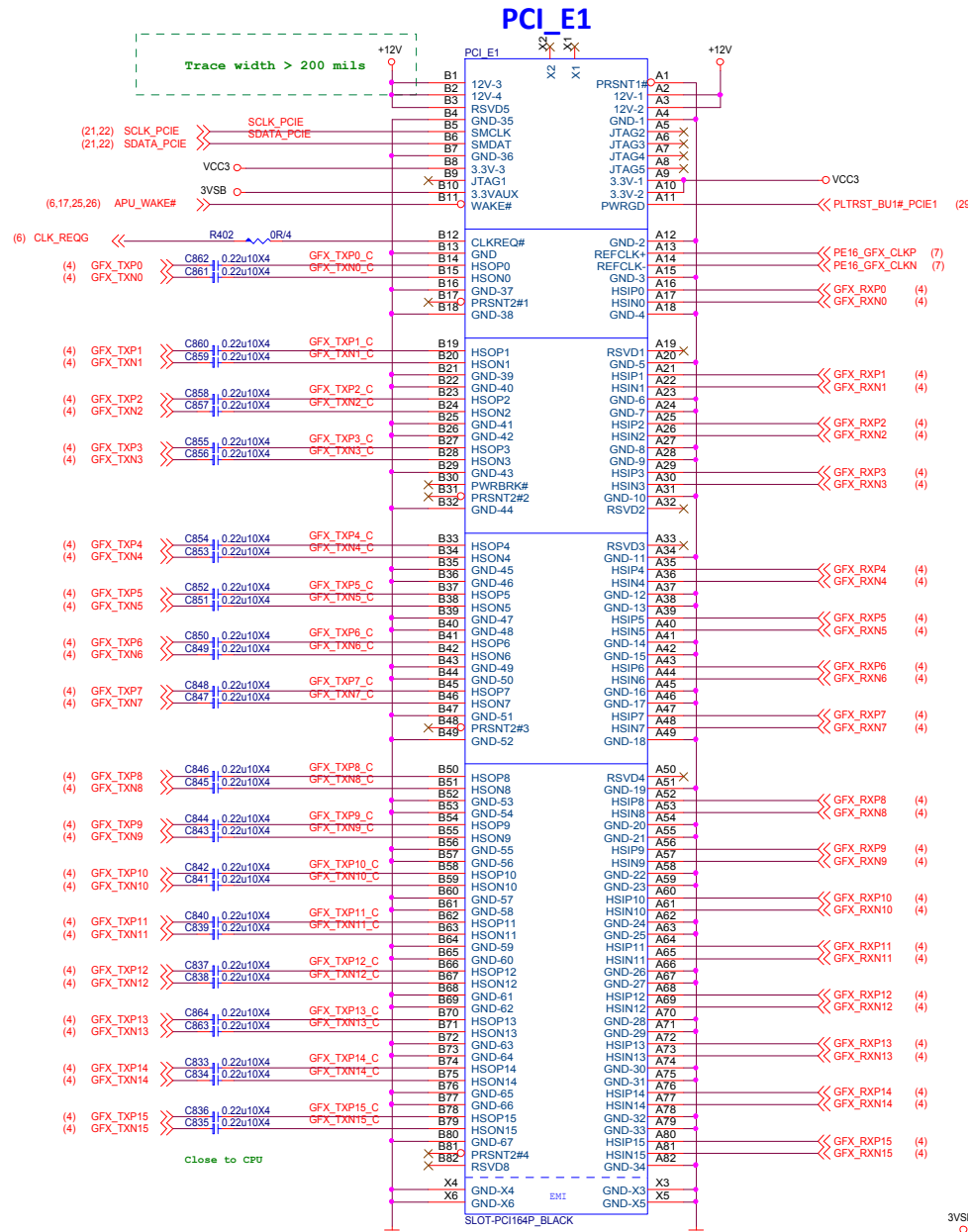
Ports	Host Controller	OC Pins Mapped
USB 3.2 Port 0 - 3 and USB 2.0 Port 0 - 5	Host Controller 0 (HC0)	USB_OC0_L/AGPIO16 USB_OC1_L/AGPIO17
USB 3.2 Port 4 - 7 and USB 2.0 Port 6 - 11	Host Controller 1 (HC1)	USB_OC2_L/AGPIO18 USB_OC3_L/AGPIO24

Close to FCH Power Pin

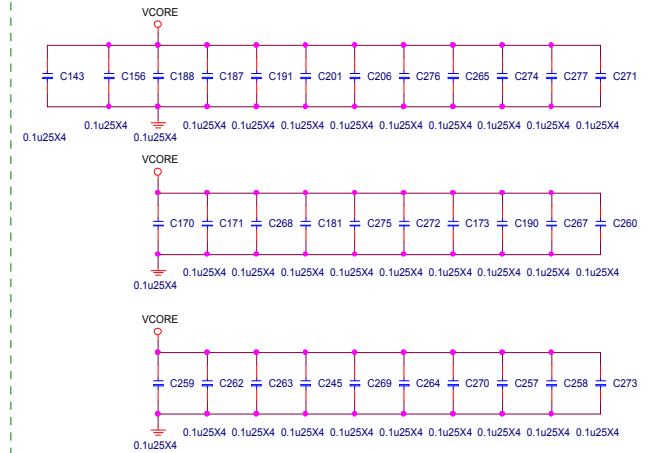




PCI EXPRESS x16 Slot

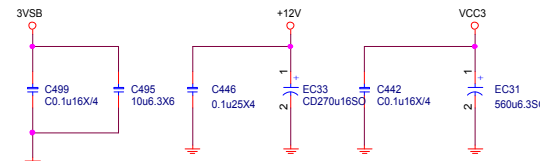


Bypass Capacitor For Across Moat



PCI Express x16 Slot

+12V	- 5.5A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA

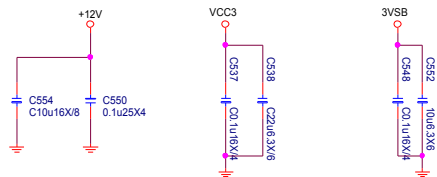
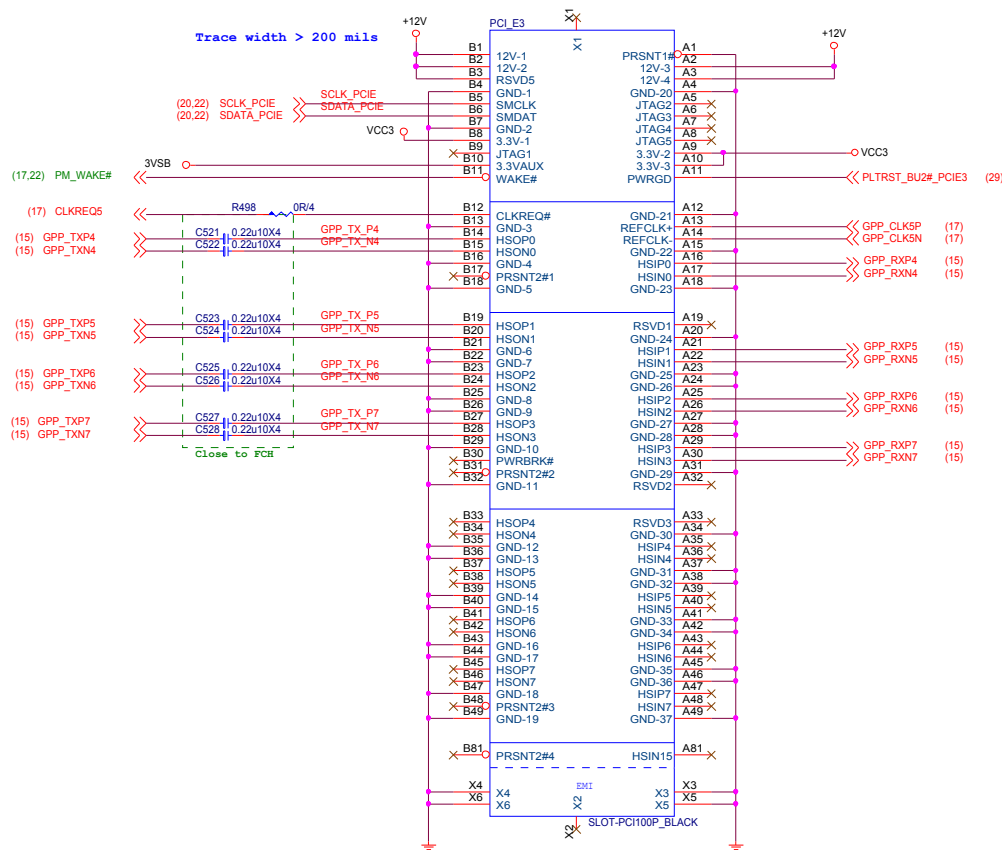


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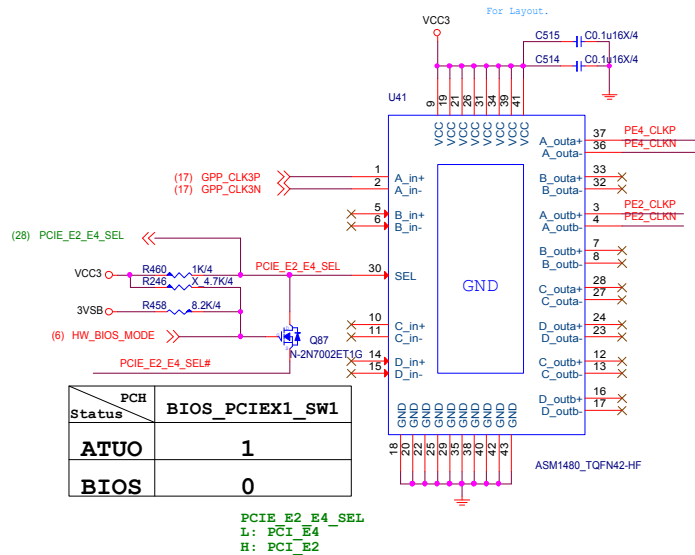
MS-7C37

Size	Document Description	Rev
Custom	PCI E1 (X16)	2.2
Date:	Thursday, July 16, 2020	Sheet 20 of 75

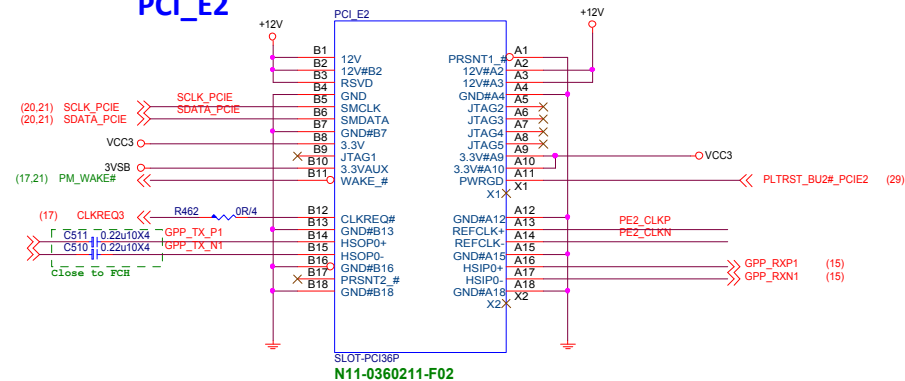
PCI_E3 X4



PCI Express x4 Slot *1		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

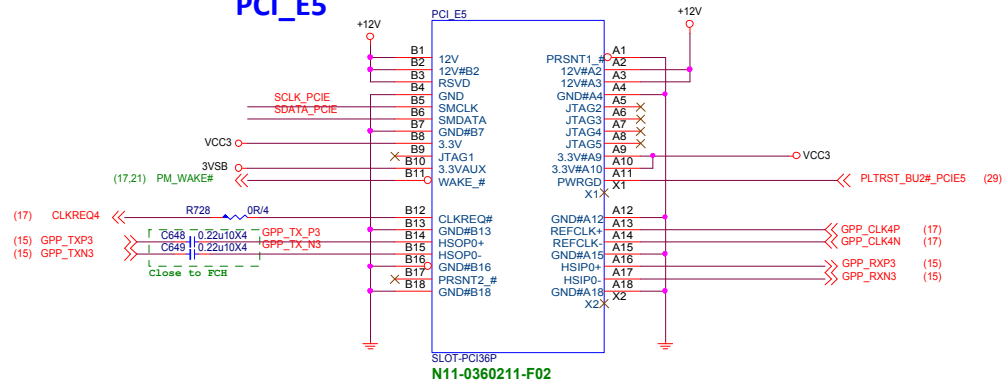


PCI_E2

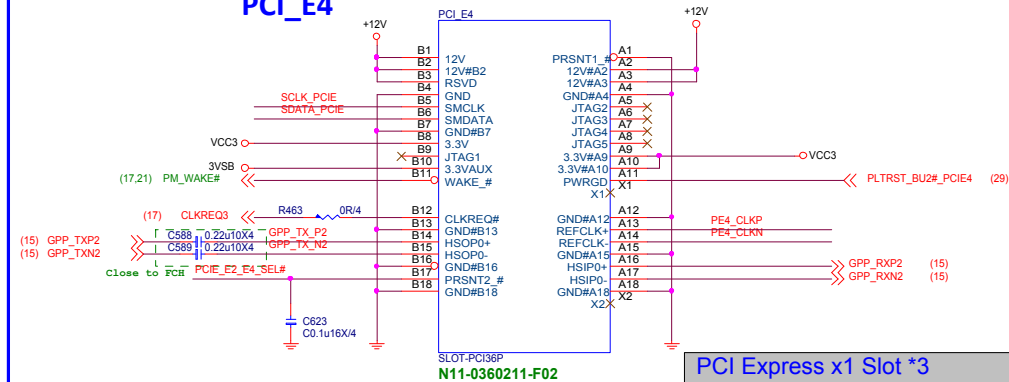


PCIE_E2 & PCIE_E4互切, PCIE_E2 & PCIE_E4同时有PCIE device 以PCIE_E4 优先

PCI_E5



PCI_E4



PCI Express x1 Slot *3

+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1125mA
+3V3_S5 (no wake)	- 60mA



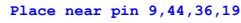
MICRO-STAR INT'L CO.,LTD

MS-7C37

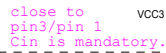
Size	Document Description	Rev
Custom	PCIE Switch PCI_E2 / E4 / E5 (X1)	2.2
Date: Thursday, July 16, 2020	Sheet 22 of 75	

1.2V delay from 3.3V 90% > 0ms

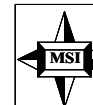
	3.3V	1.25V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



SATA_SPI_DO don't need pull up
(integrated pull-up)
or pull down for Asmedia
recommendation.
Asmedia suggest that we use
spinup by s/w mode for MB or
PCI-E Card.

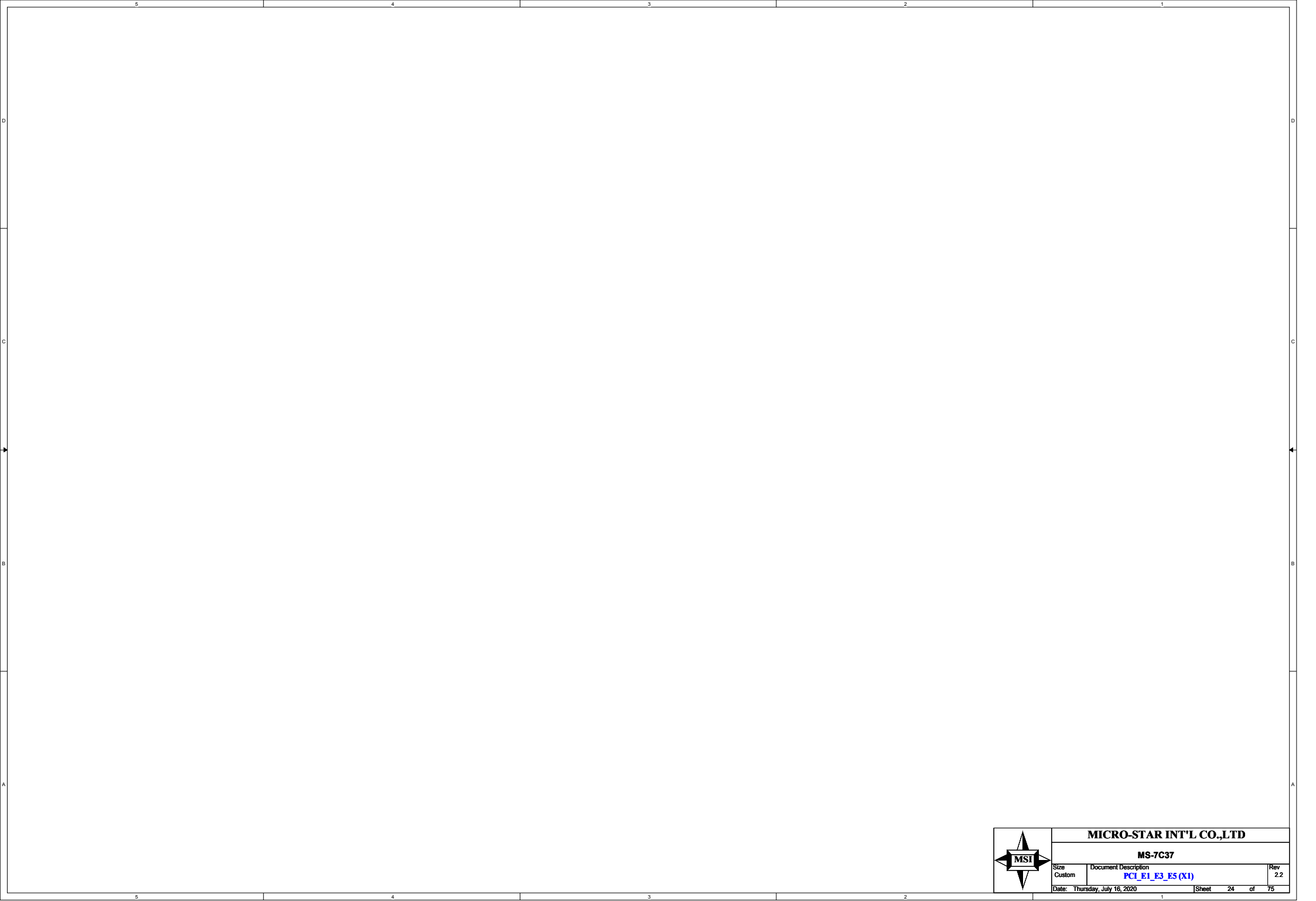


close to pin



MS-7C37

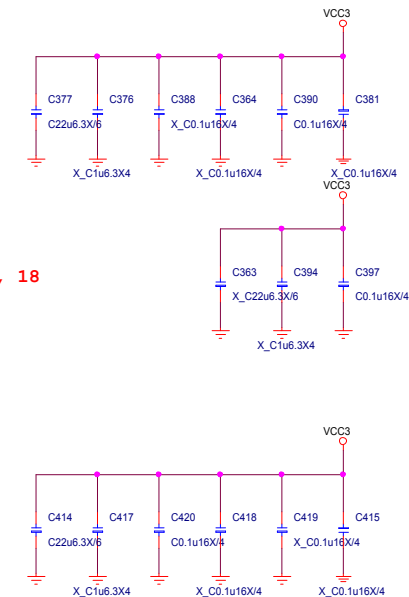
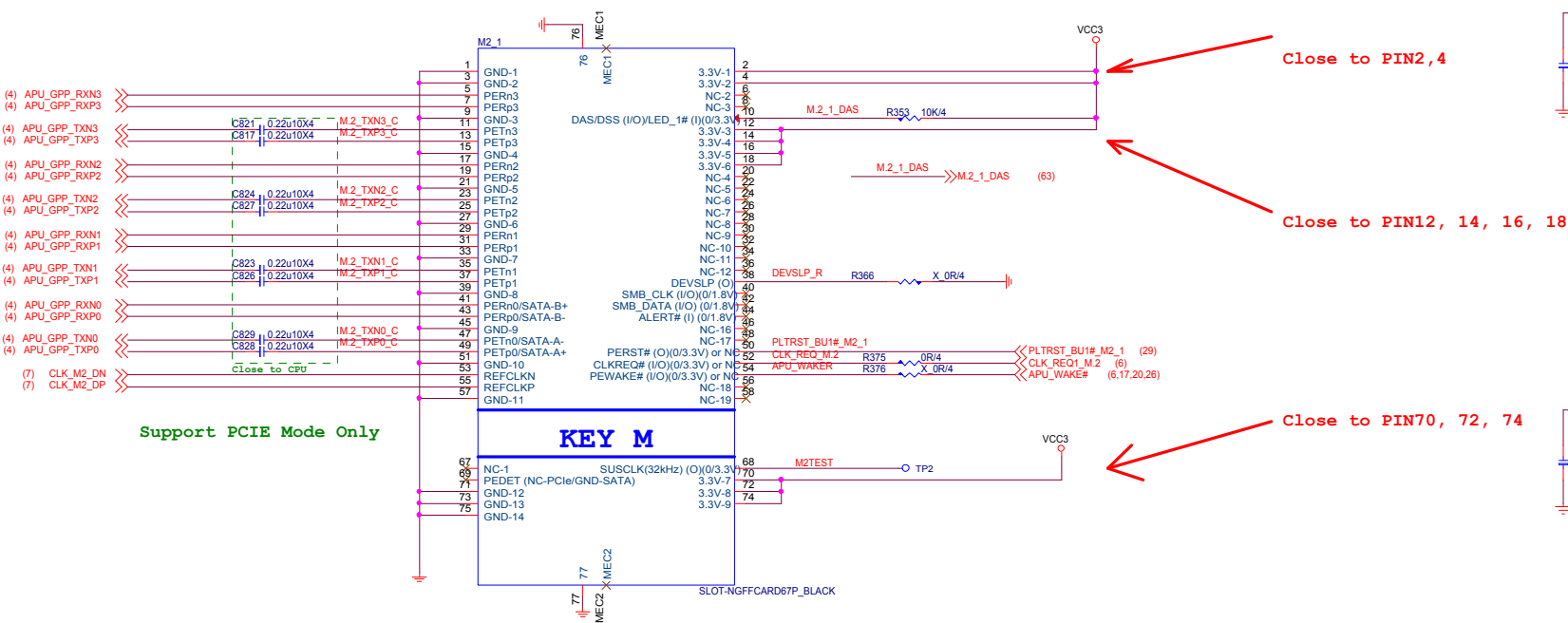
Size Custom	Document Description PCIE to SATA (ASMI061)	Rev 2.2
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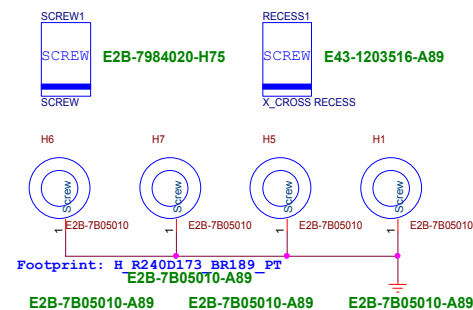
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MS-7C37		
Size Custom	Document Description PCL E1_E3_E5 (X1)	Rev 2.2
Date: Thursday, July 16, 2020	Sheet 24 of	75

M.2 1 Connector

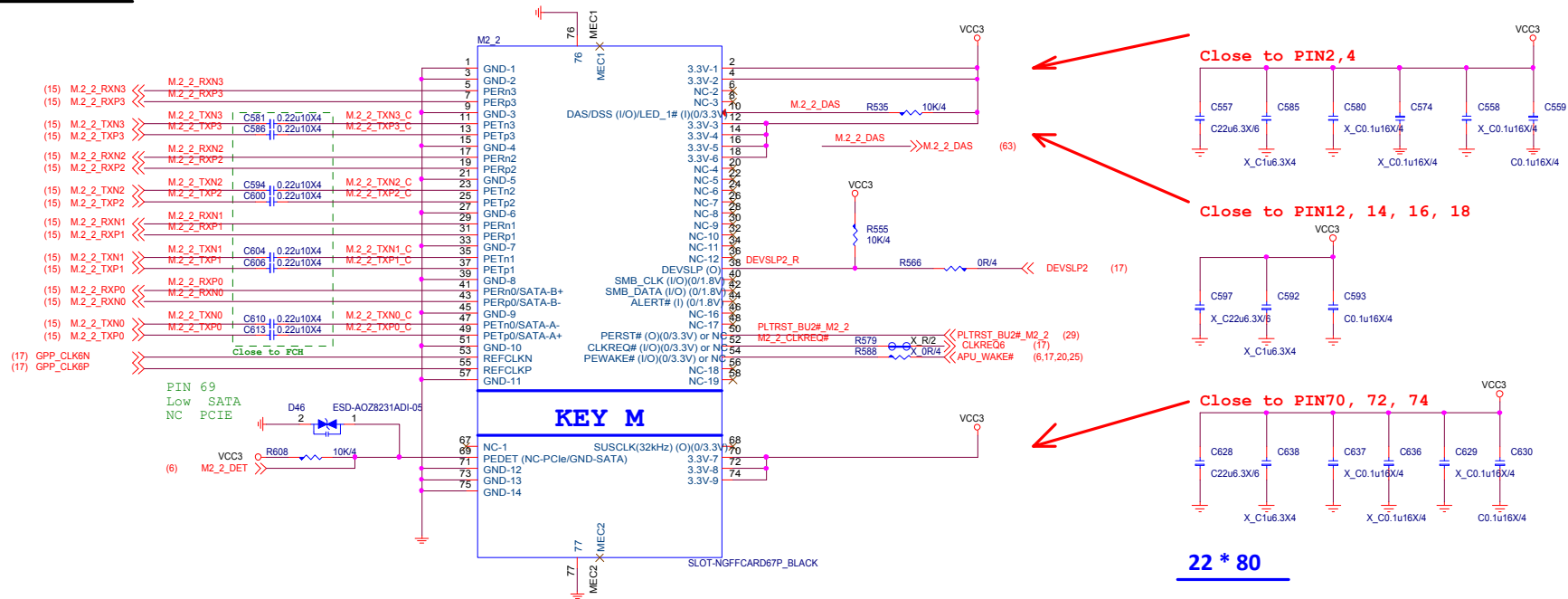
VCC3 4.25A
Max: 14W



22 * 110

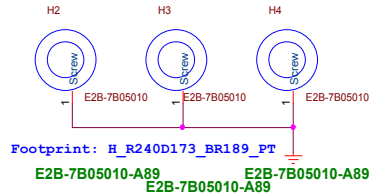
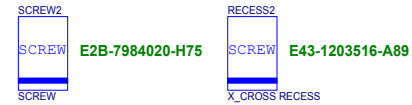


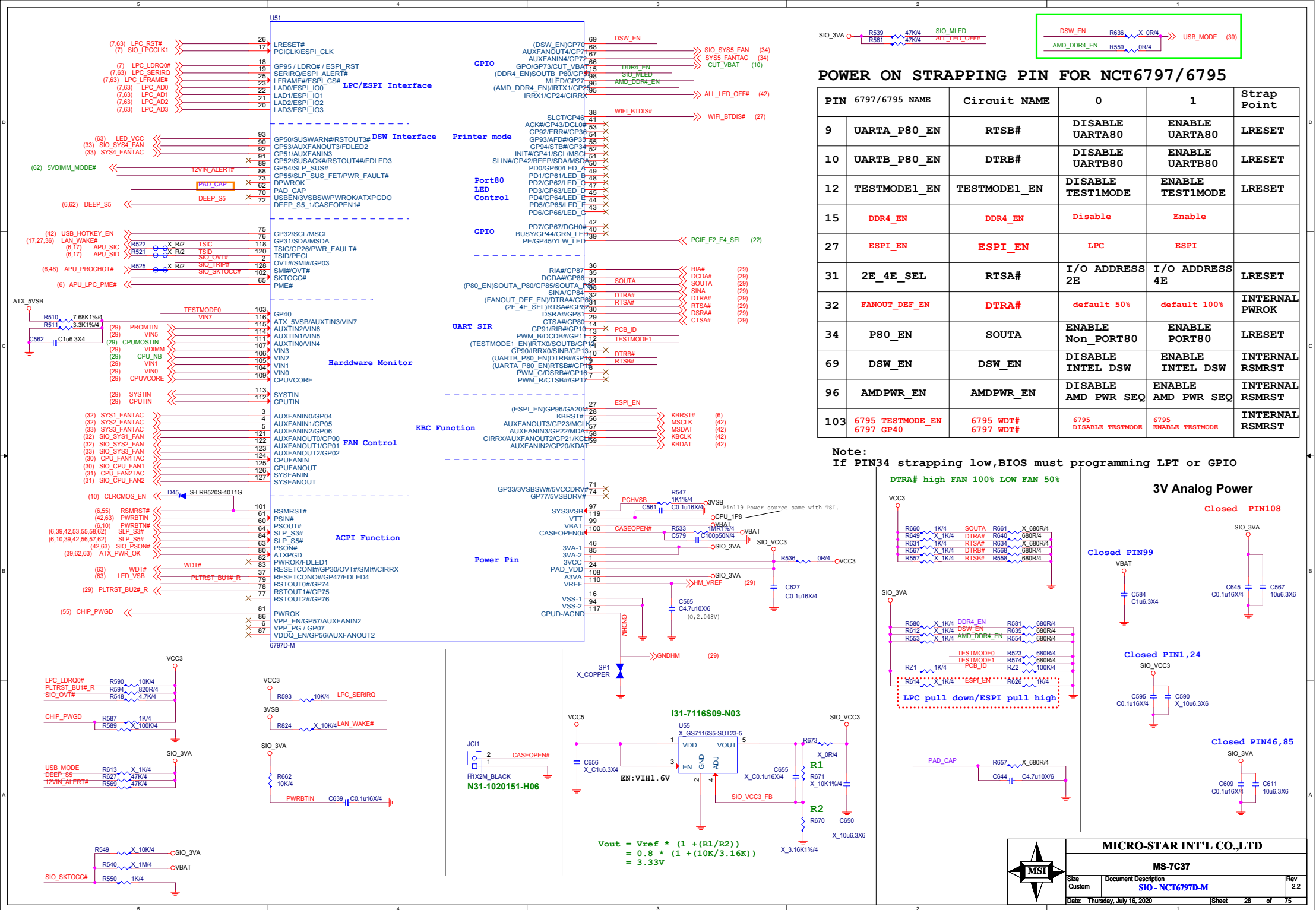
M.2 2 Connector



Support PCIE and SATA Mode

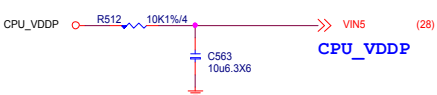
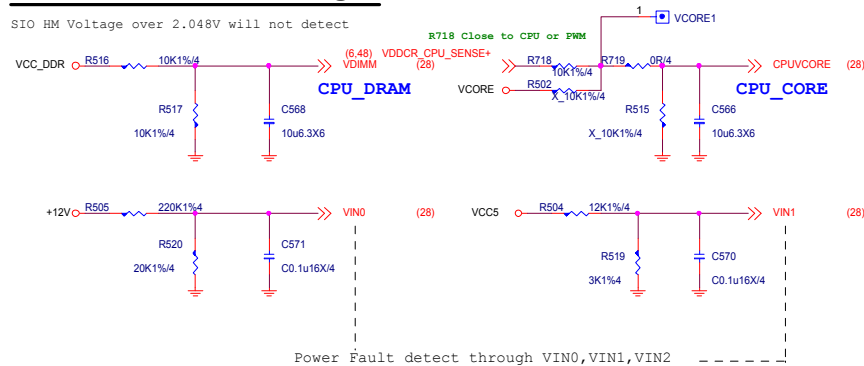
22 * 80



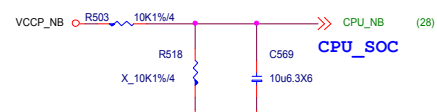


HW Monitor - Voltage

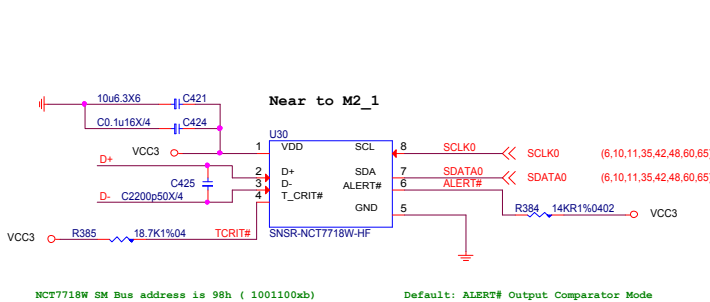
SIO HM Voltage over 2.048V will not detect



Inform BIOS disable VIN2 with Power Fault

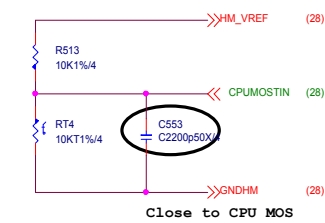
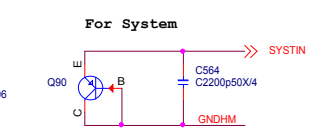
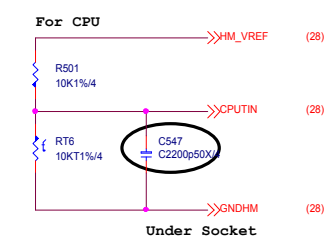


NCT7718W

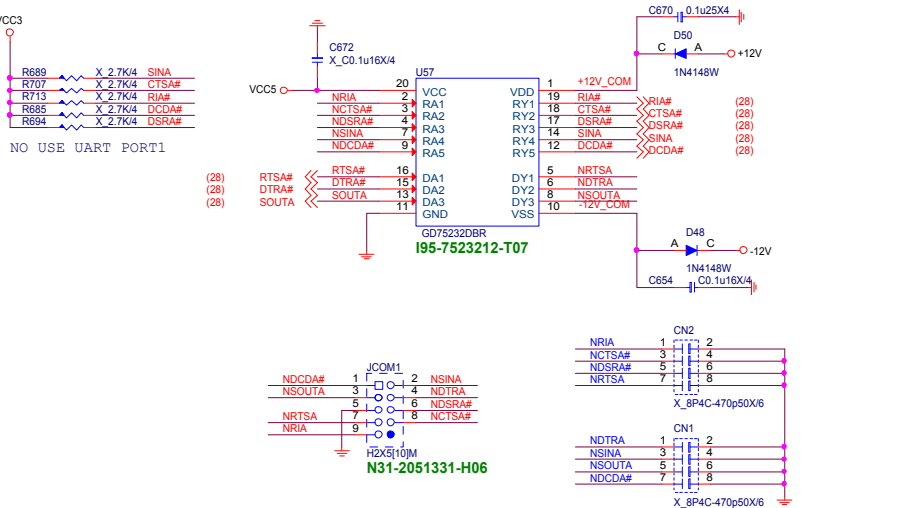


TEMPERATURE (°C)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	77	87	97	107	117
	79	89	99	109	119
	81	91	101	111	121
	83	93	103	113	123
	85	95	105	115	125

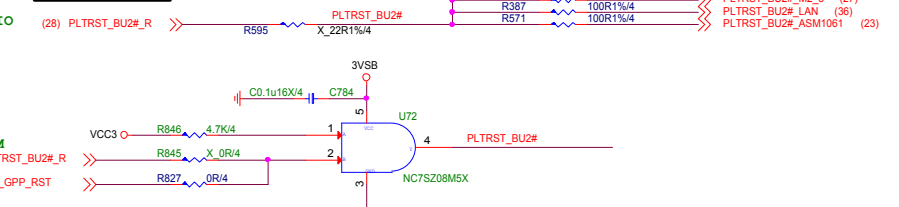
TEMP SENSOR



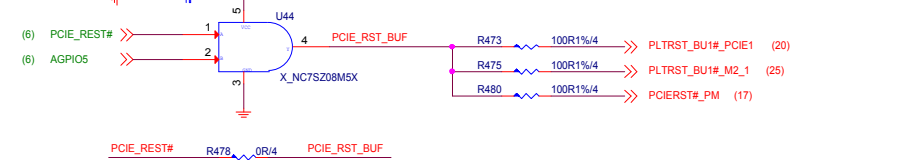
COM PORT



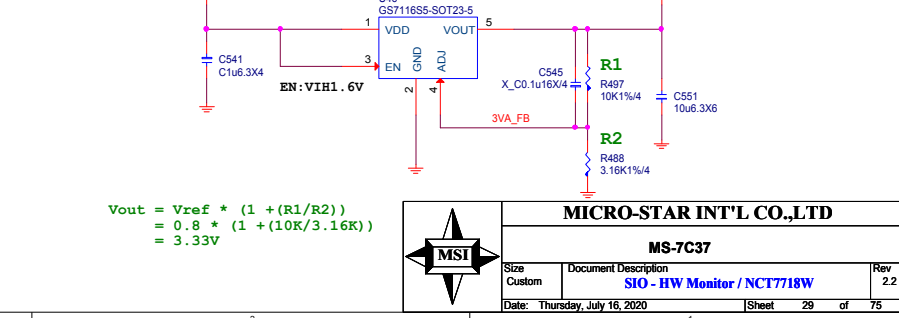
PM RESET



CPU RESET



SIO_3VA



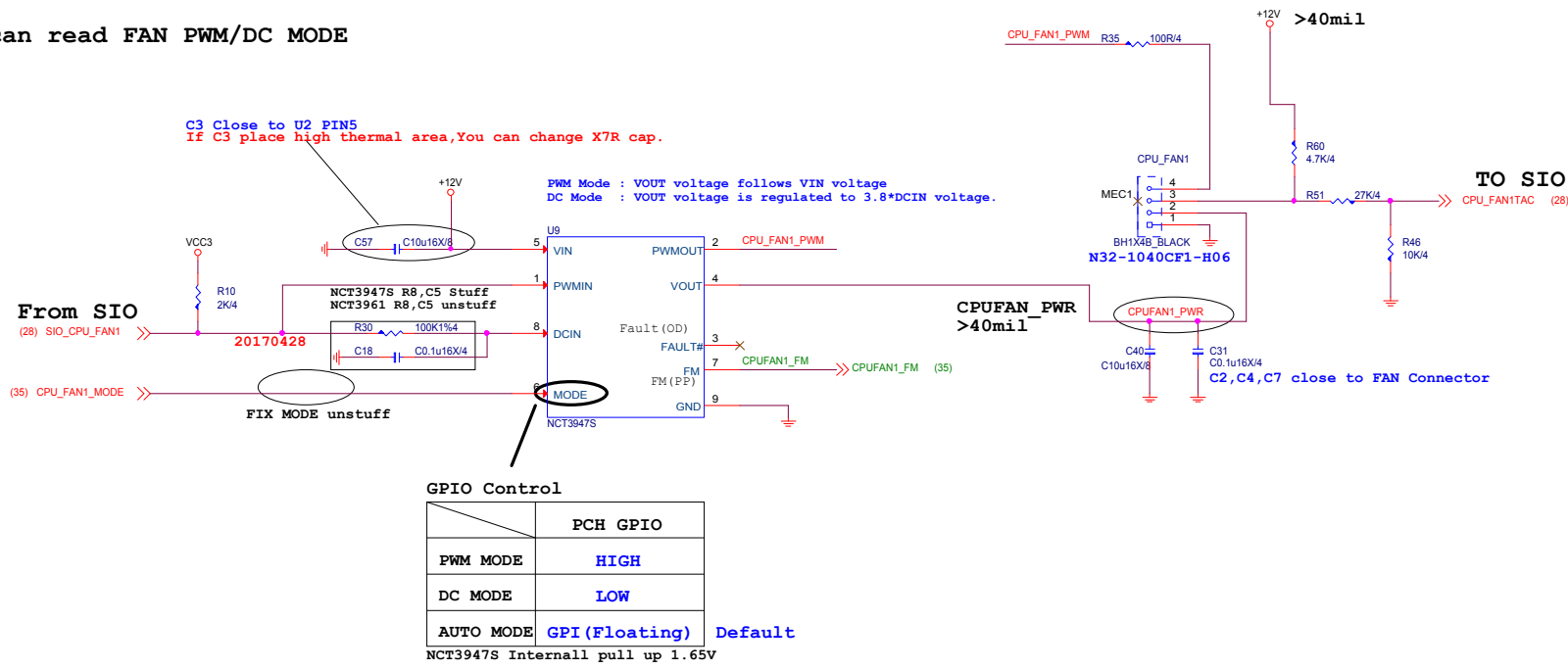
$$V_{out} = V_{ref} * (1 + (R1/R2)) = 0.8 * (1 + (10K/3.16K)) = 3.33V$$

MICRO-STAR INT'L CO.,LTD
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Size Custom Document Description **SIO - HW Monitor / NCT7718W** Rev 2.2
Date: Thursday, July 16, 2020 [Sheet 29 of 75]

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

CPUFAN1

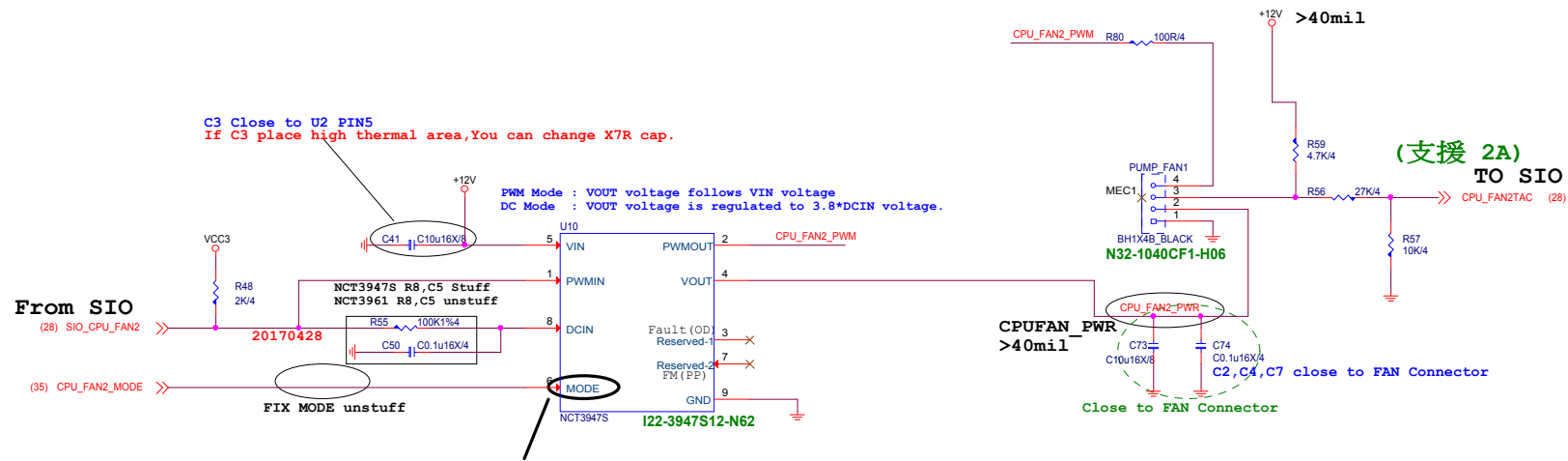
- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

PUMPFAN1

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

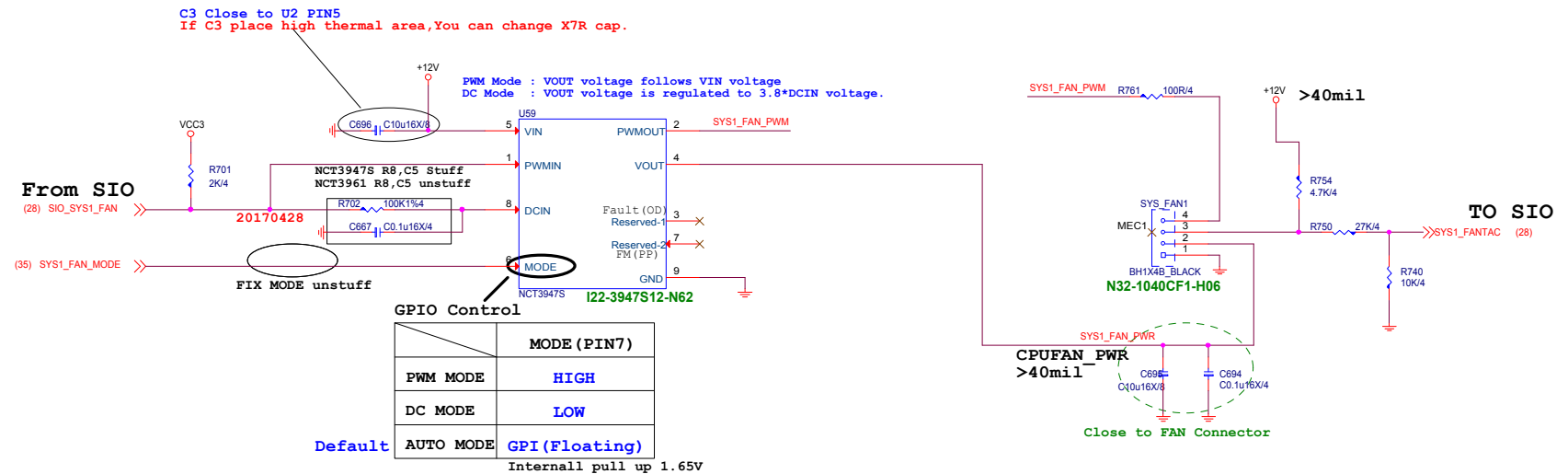
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating) Default

NCT3947S Internall pull up 1.65V

SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

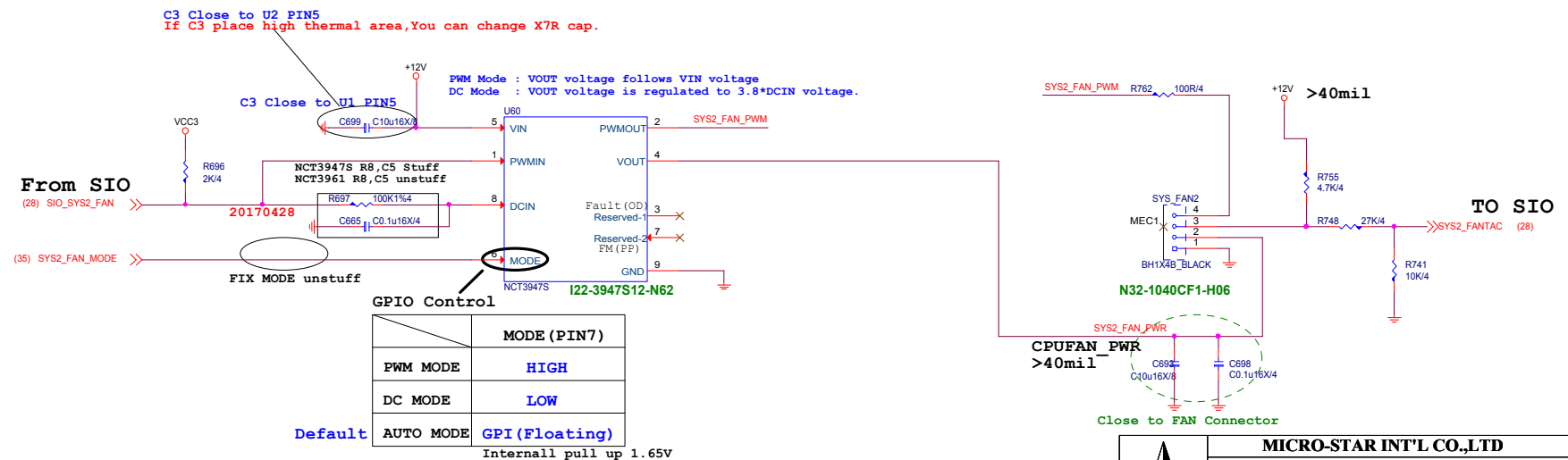
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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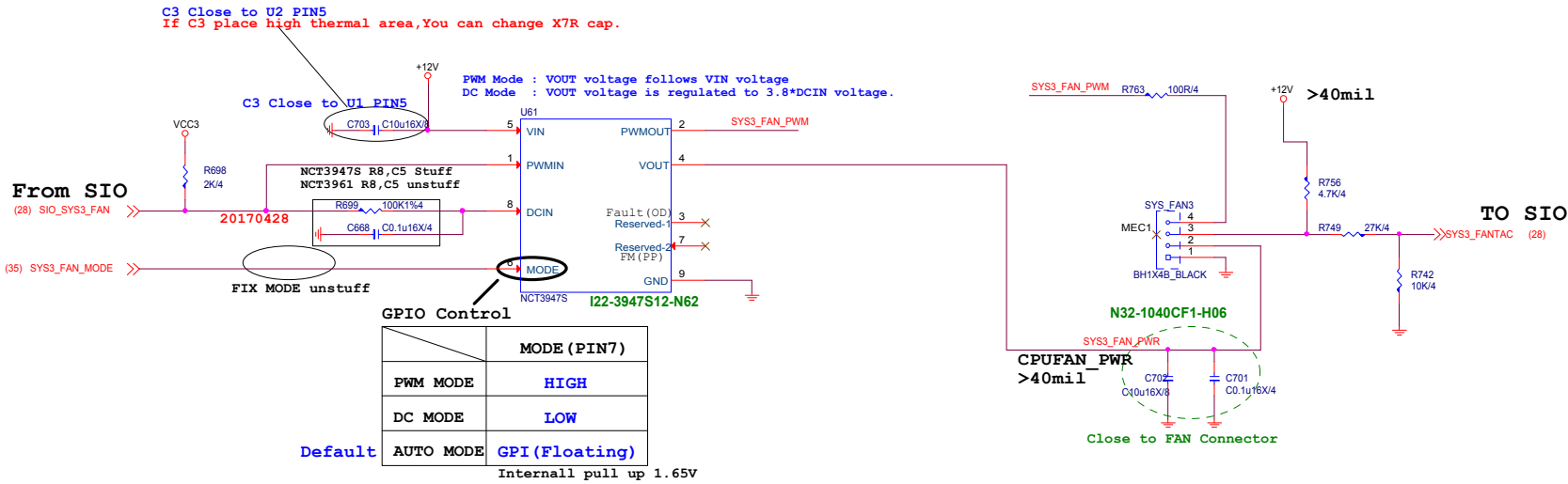
MS-7C37

Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN1/2	2.2
Date:	Thursday, July 16, 2020	Sheet 32 of 75

SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

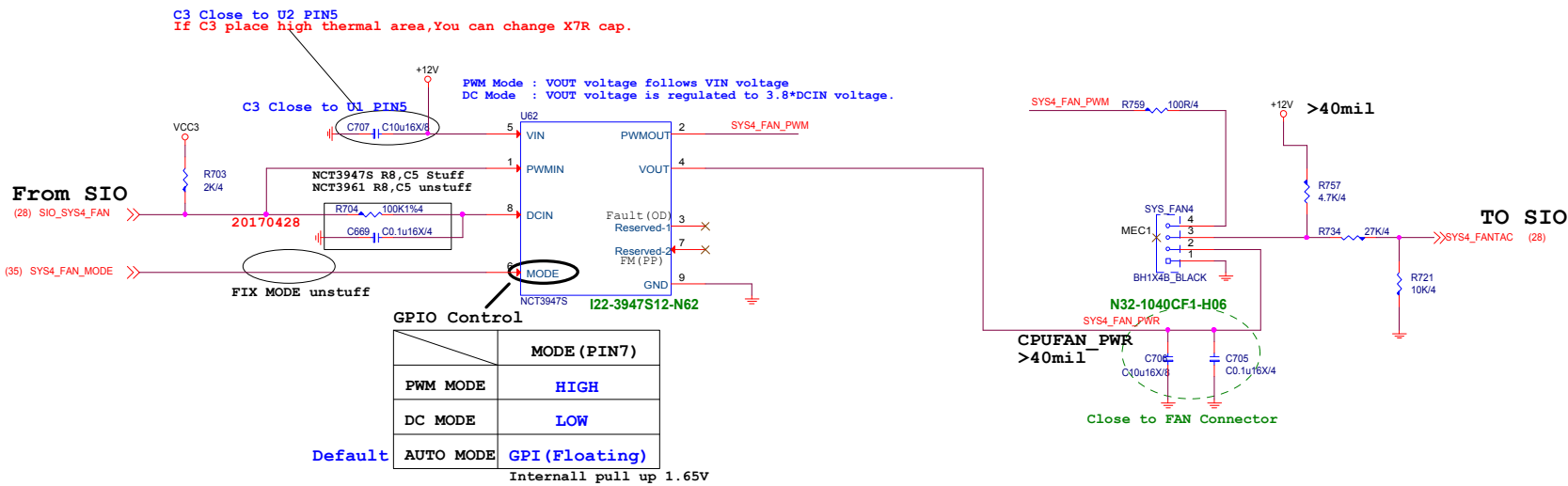
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

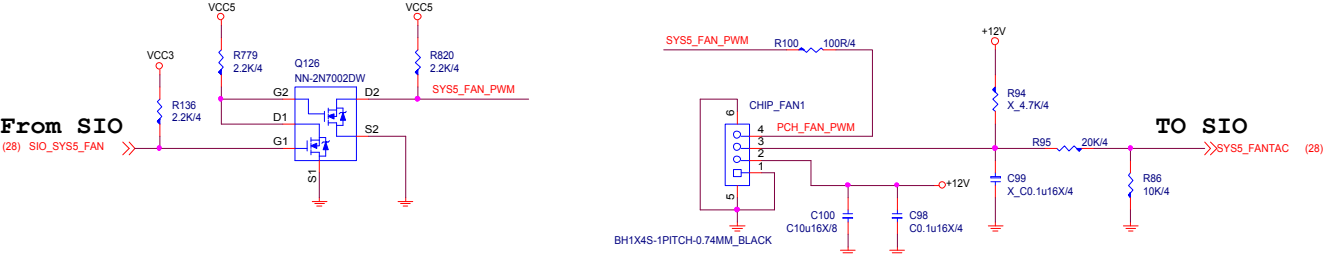


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN3/4	2.2
Date: Thursday, July 16, 2020		
Sheet 33 of 75		

PCH_FAN



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Size Custom	Document Description PCH_FAN	Rev 2.2
Date: Thursday, July 16, 2020		Sheet 34 of 75

By PM Define FAN name

SHOW FAN FAULT USE	FAN
GP10	CPUFAN1
GP11	CPUFAN2 PUMPFAN

BIOS SHOW FAN FAULT Information USE
Default GPI

BIOS SHOW FAN MODE Information USE
Default GPI

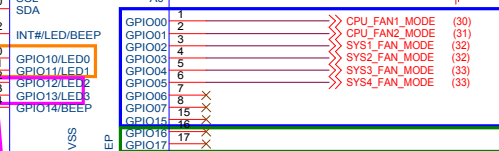
use avoid S5 leakage



By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

slave address :
Write 4CH
Read 4DH



By PM Define FAN name

LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

Default GPI

USE LED OFF & LED BLINK

By PM Define FAN name

FAN MODE USE	FAN
GP00	CPUFAN1
GP01	CPUFAN2 PUMPFAN
GP02	SYSFAN1
GP03	SYSFAN2
GP04	SYSFAN3
GP05	SYSFAN4
GP06	SYSFAN5
GP07	EXT SYS FAN1
GP15	EXT SYS FAN2



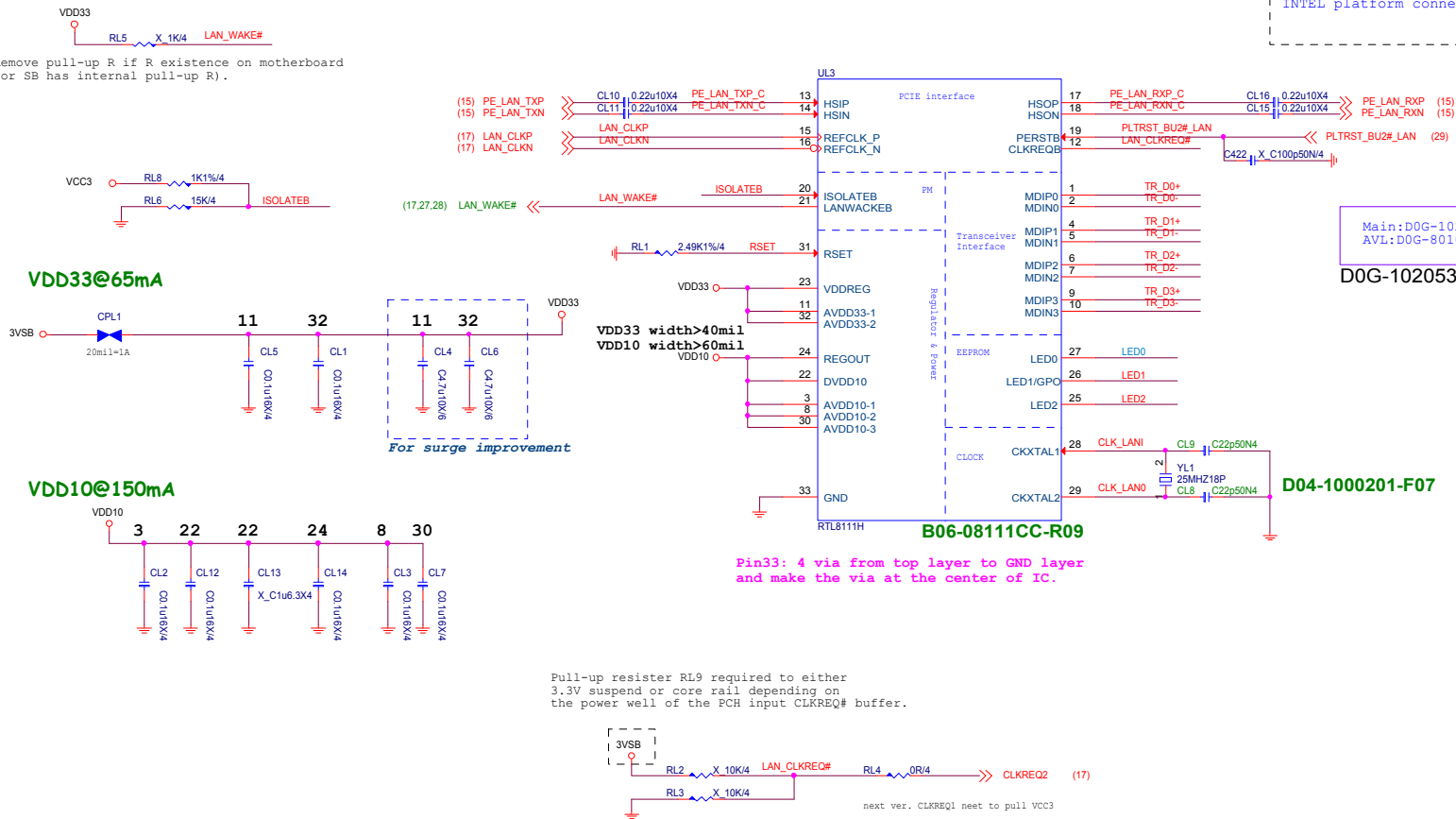
MICRO-STAR INT'L CO.,LTD

MS-7C37

Size	Document Description	Rev
Custom	FAN GPIO NCT5635	2.2
Date:	Thursday, July 16, 2020	Sheet 35 of 75

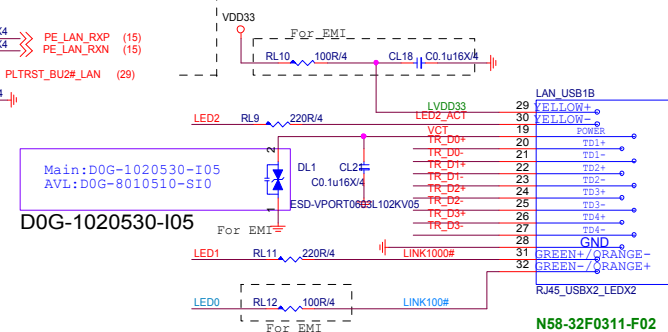
RTL8111H Giga LAN

Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).

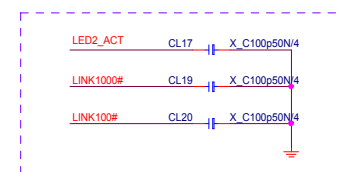


PIN19:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#.

LAN Connector

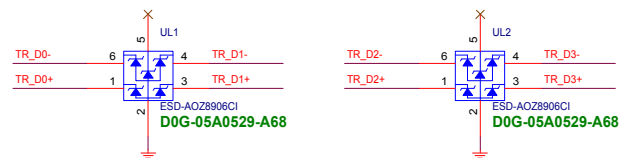


For EMI



ESD Protect close to connector

D0G-0200529-A68
D0G-0100619-I05



8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

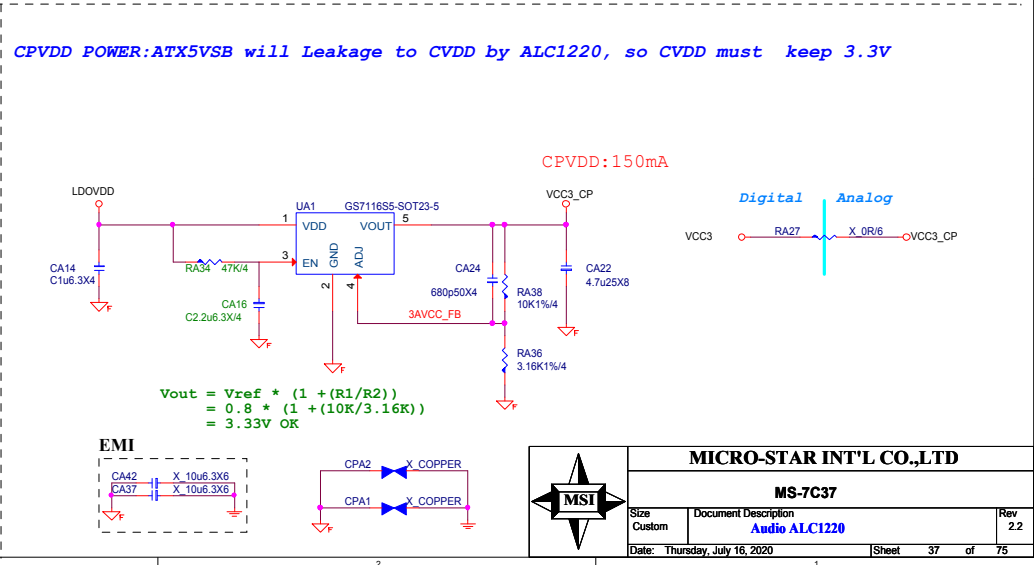
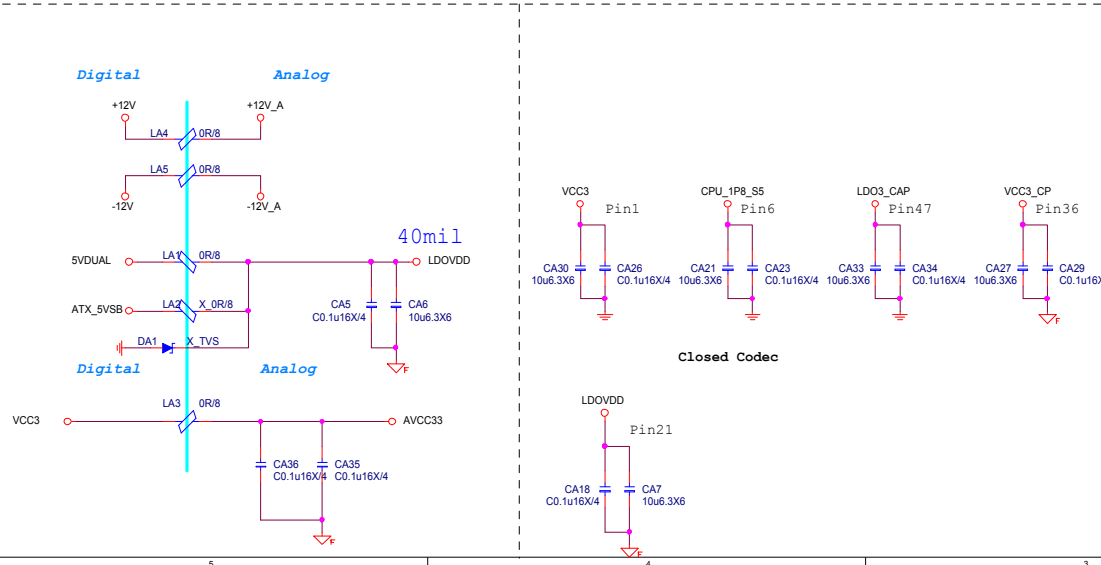
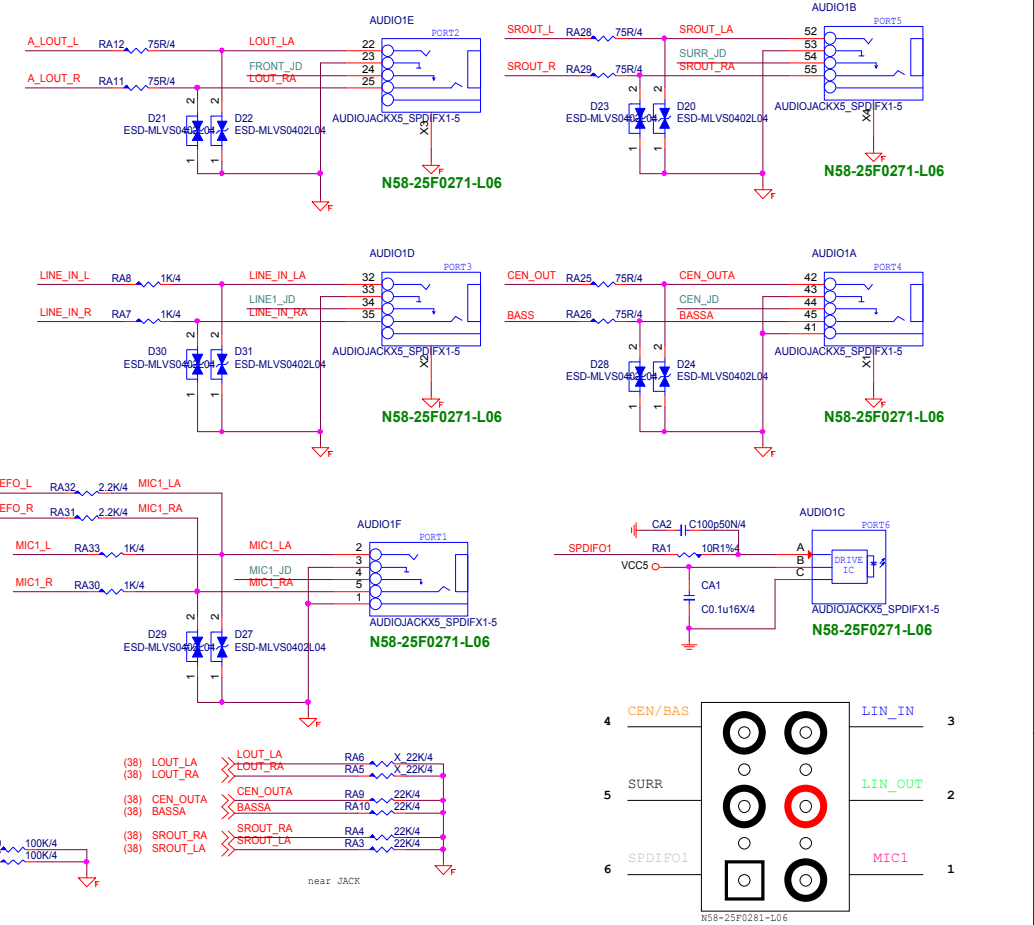
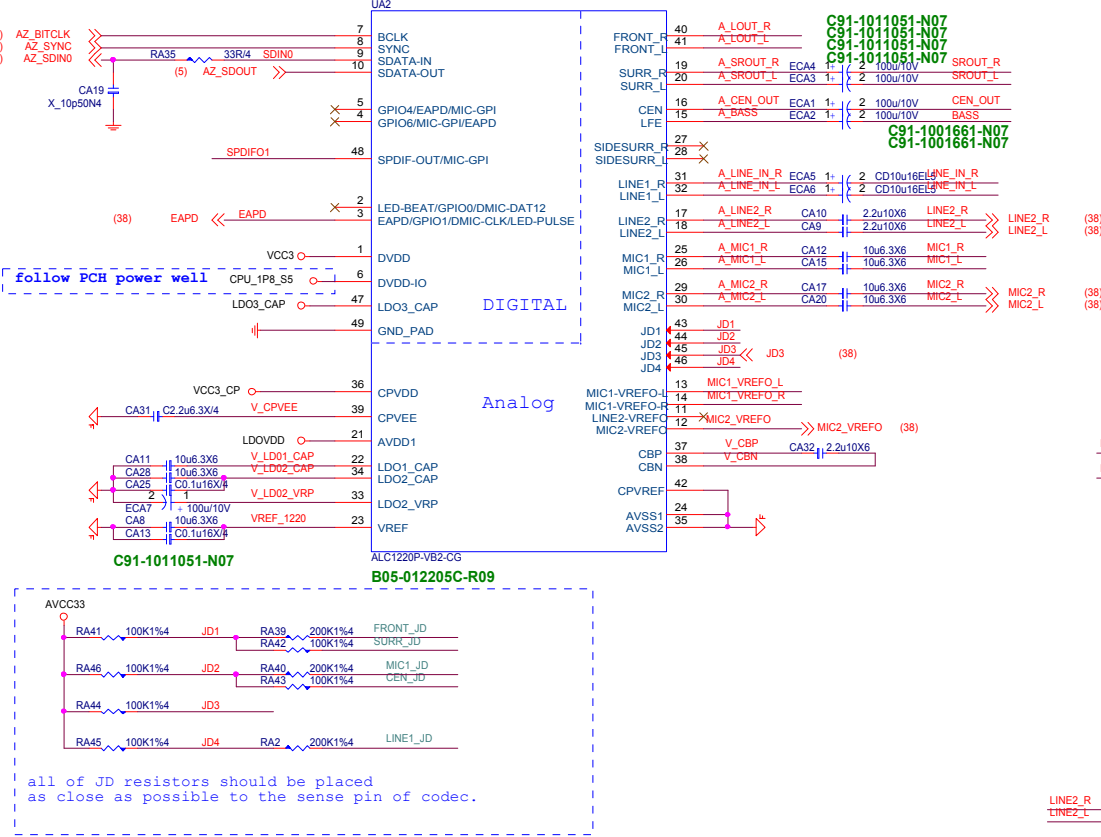



MICRO-STAR INT'L CO.,LTD

MS-7C37

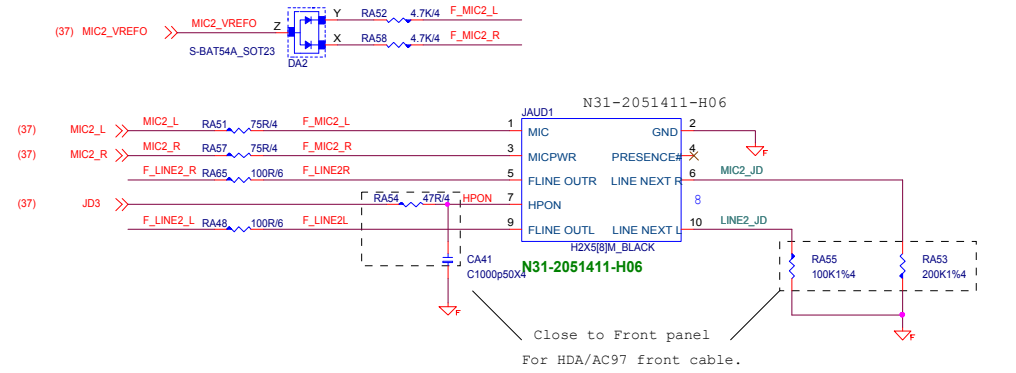
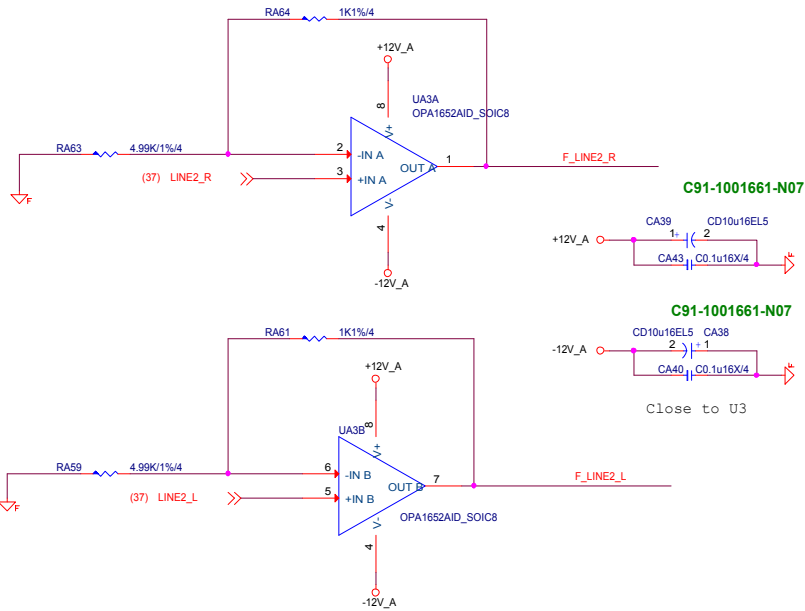
Size	Document Description	Rev
Custom	LAN - I211AT	2.2
Date: Thursday, July 16, 2020	Sheet 36 of 75	

ALC1220P-VB2_48PIN





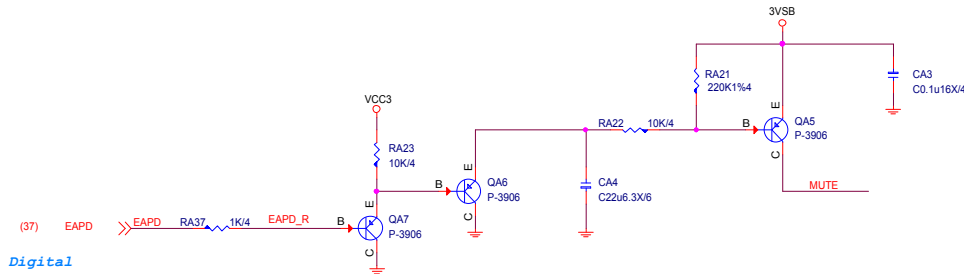
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size	Document Description	Rev
Custom	Audio ALC1220	2.2
Date: Thursday, July 16, 2020		Sheet 37 of 75



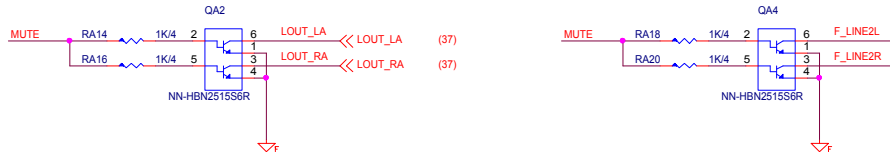
Close to Jack
ESD protect



Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)

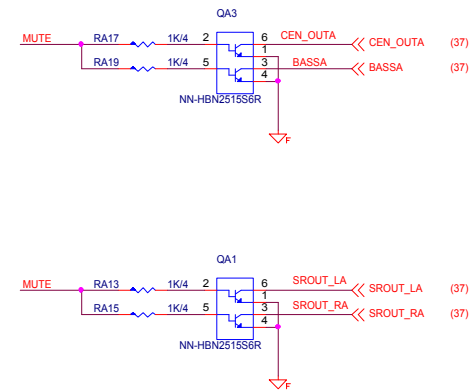


Analog

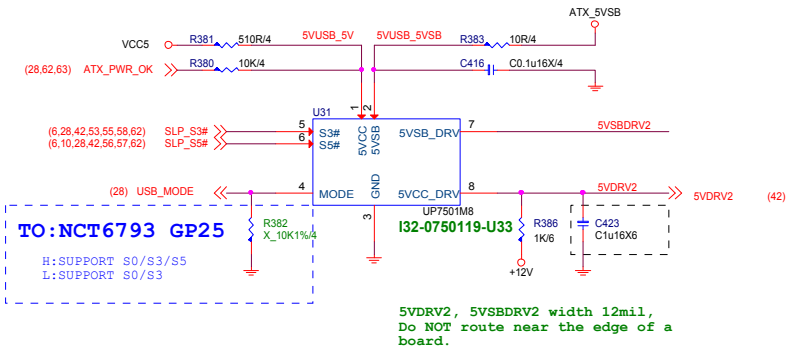


Audio moat is transparent and width 40mil

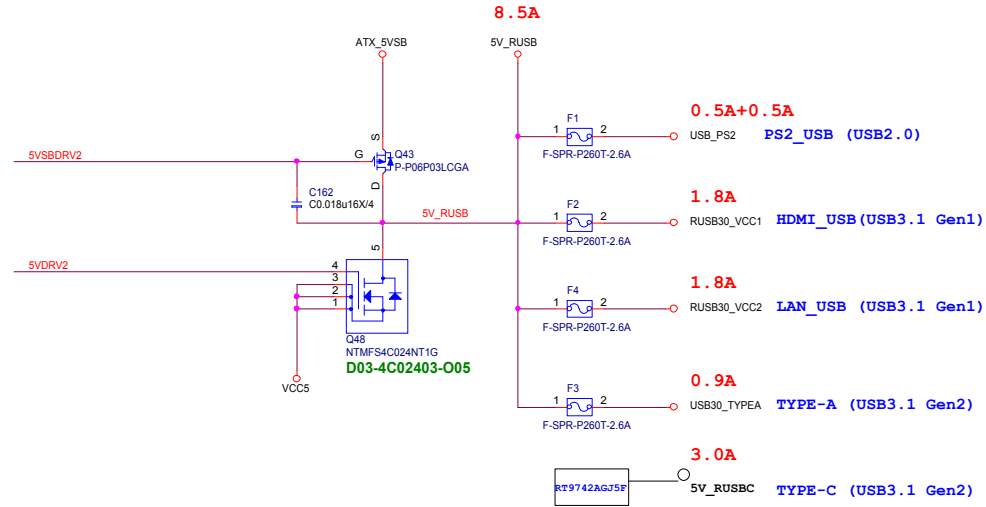
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SROUT_LA, SROUT_RA, CEN_OUTA, BASSA to TVS)



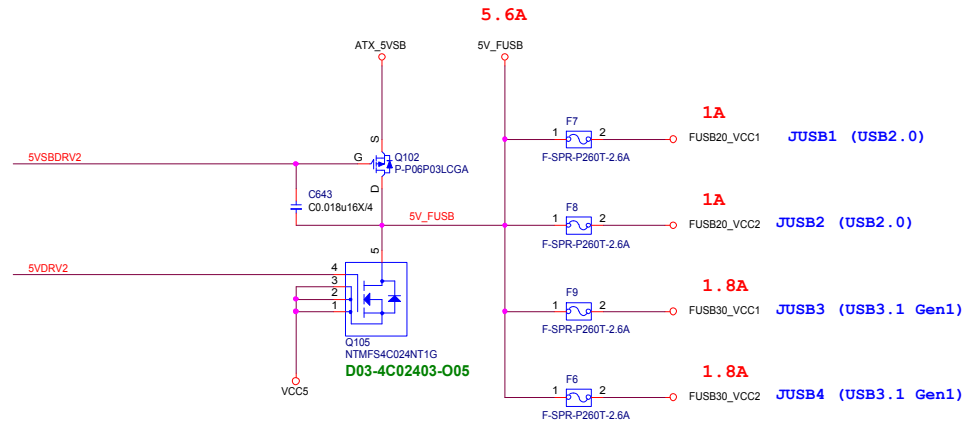
USB Power



Rear USB Port Power



Front USB Port Power

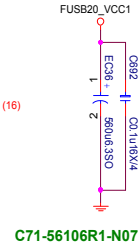
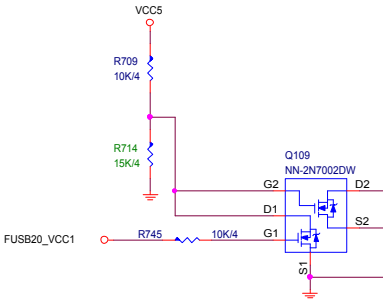
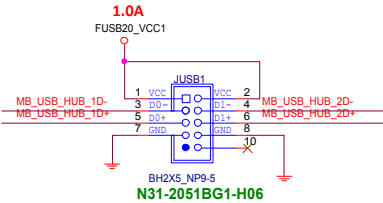
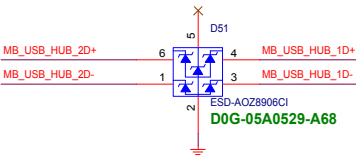
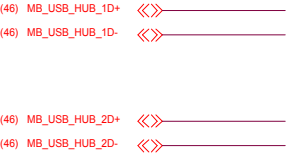


MICRO-STAR INT'L CO.,LTD

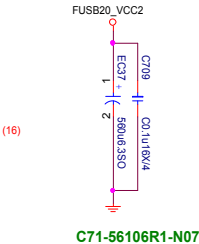
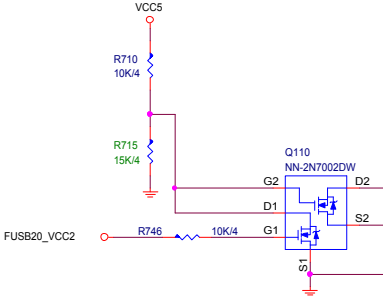
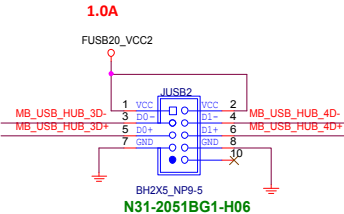
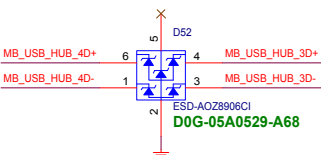
MS-7C37

Size Custom	Document Description USB Power - UP7501	Rev 2.2
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Front USB2.0 (JUSB1)

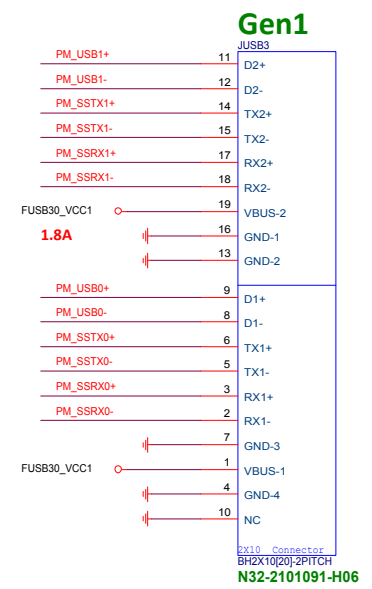
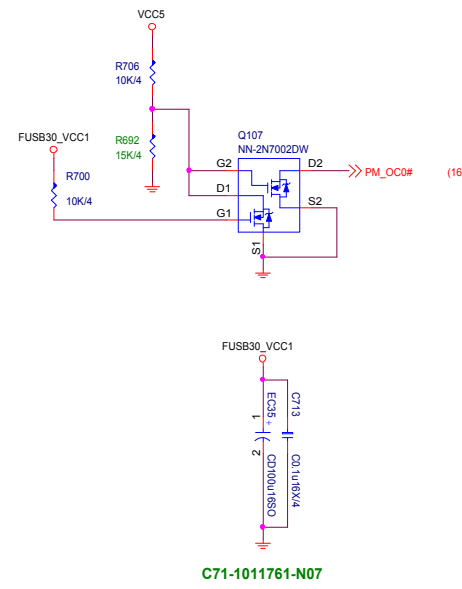
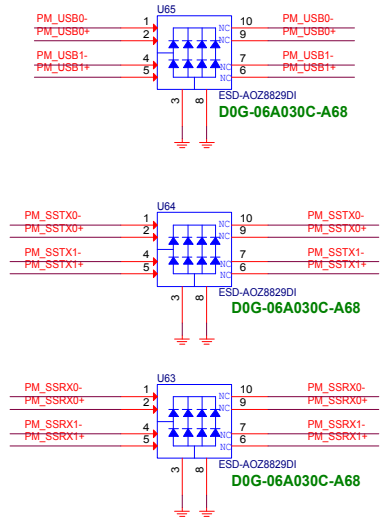
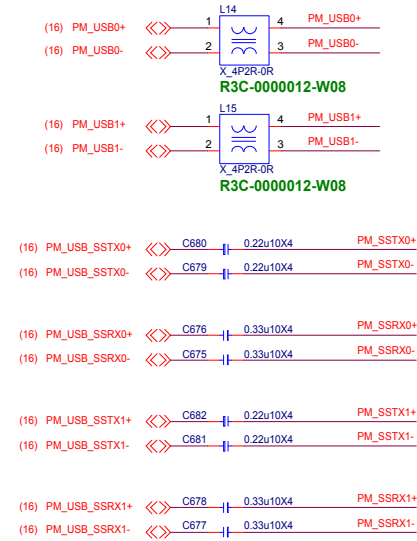


Front USB2.0 (JUSB2)

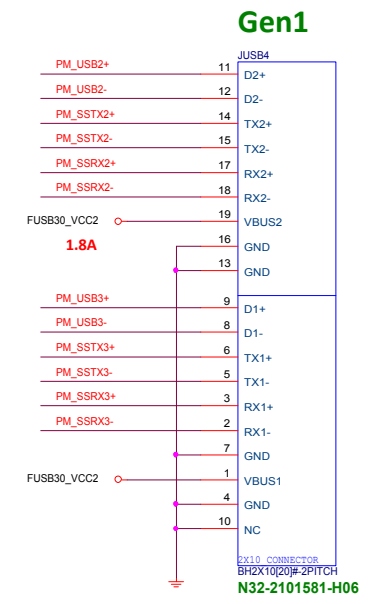
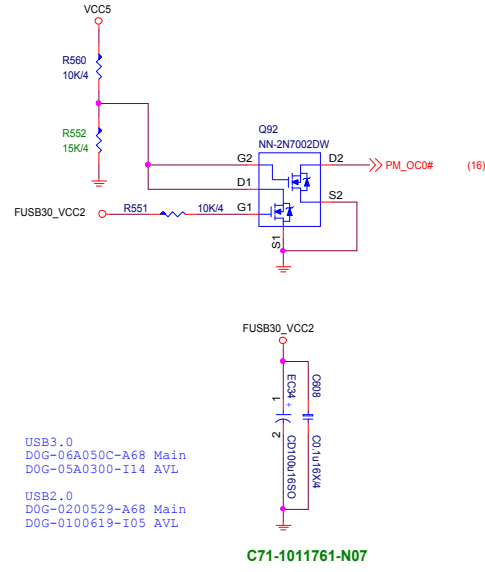
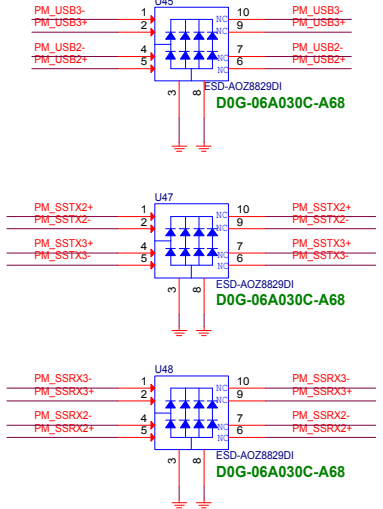
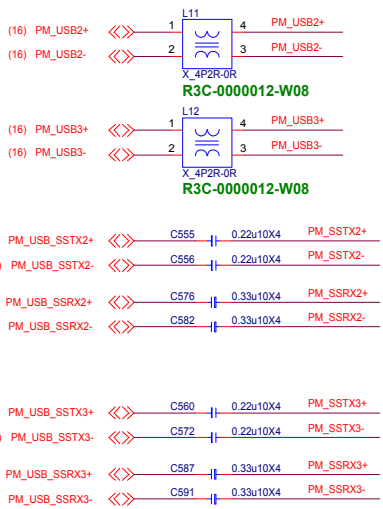


MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size	Document Description	Rev
Custom	Front USB2.0 Header	2.2
Date: Thursday, July 16, 2020		
Sheet 40 of 75		

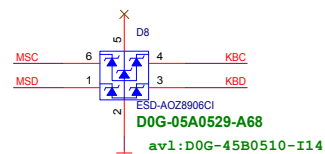
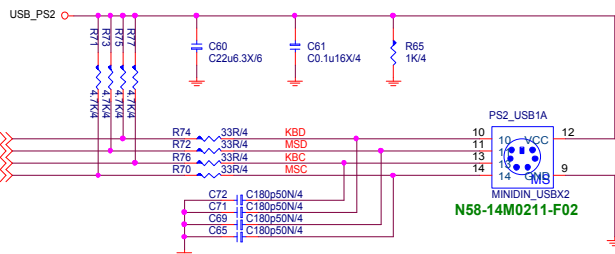
Front USB3 180° BOX Header(JUSB3)



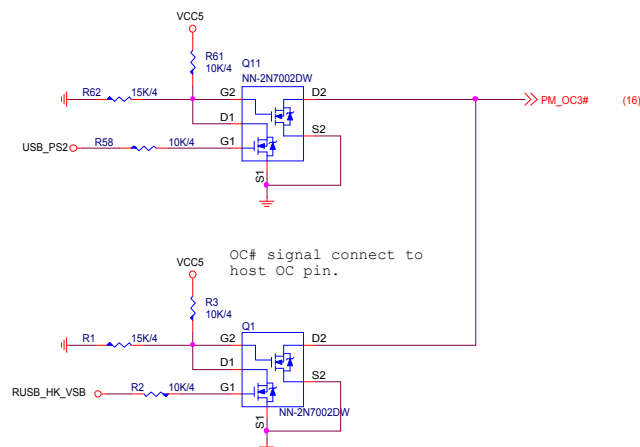
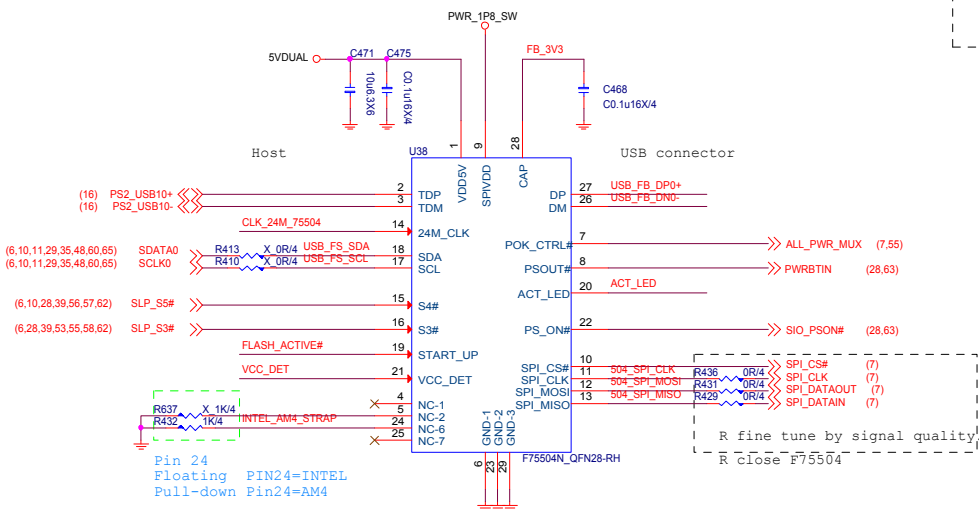
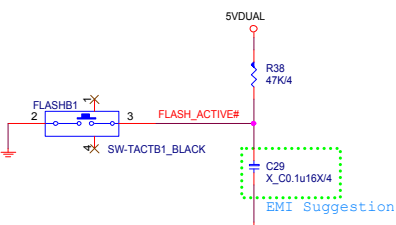
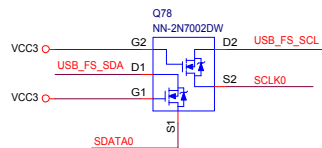
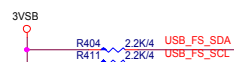
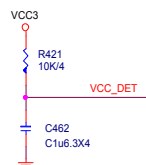
Front USB3 90° BOX Header(JUSB4)



5V@1A

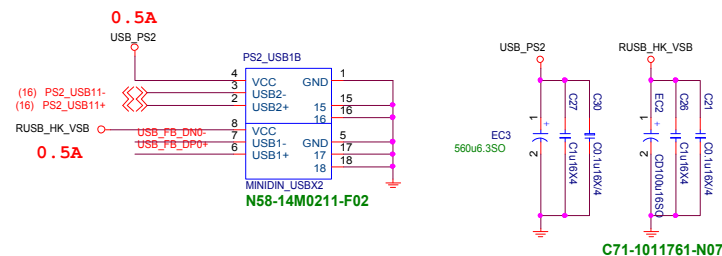
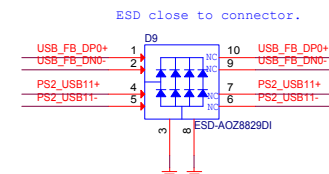
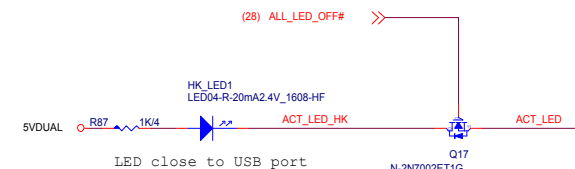


F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

[illegible]

default=> GPI
Register POWER Well
=> VSB or VBAT

(28) USB_HOTKEY_EN



MS-7C37

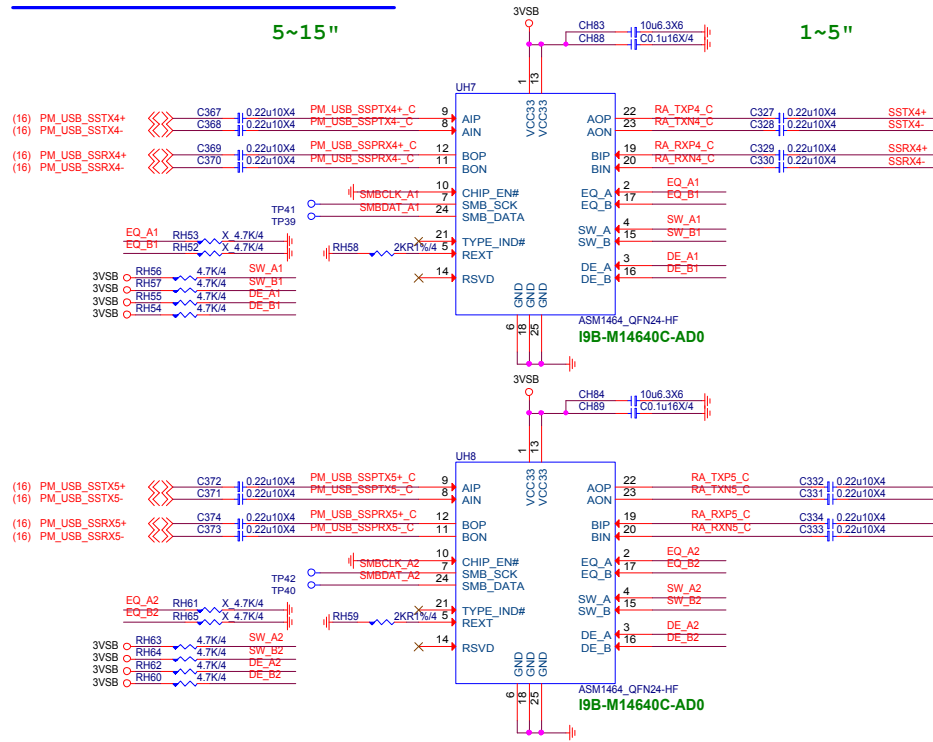
Size Custom	Document Description Rear USB2.0 + PS2	Rev 2.2
Date: Thursday, July 16, 2020		Sheet 42 of 75

LAN USB3.1 Gen1 Type-A

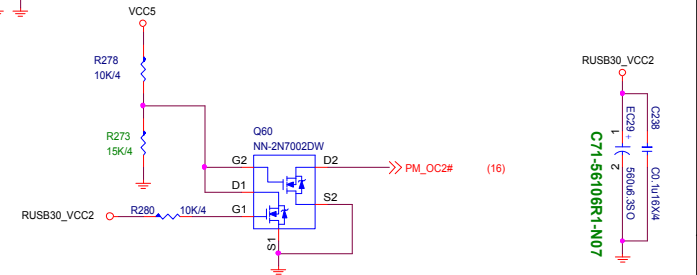
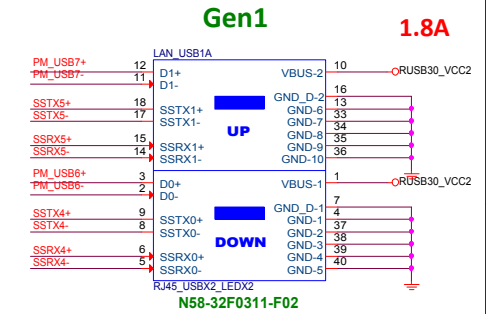
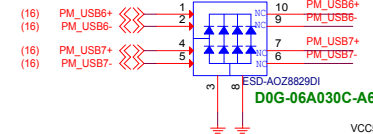
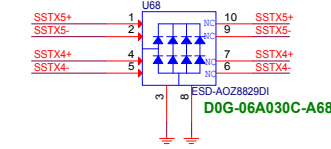
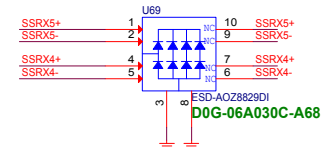
0.13A

5~15"

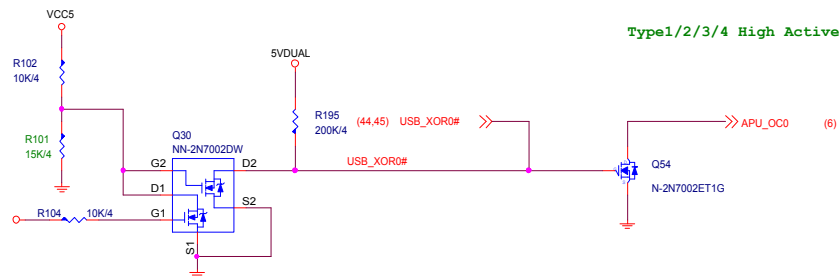
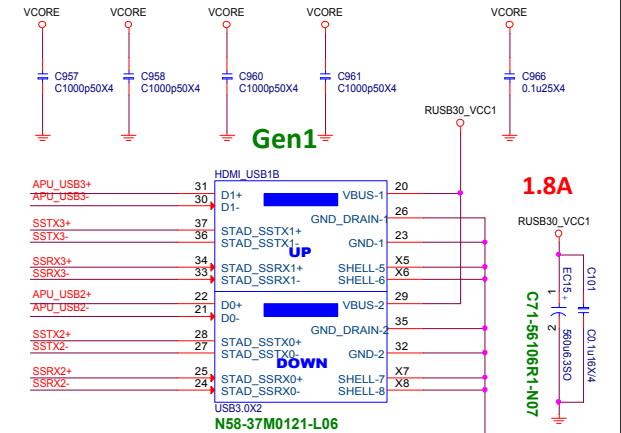
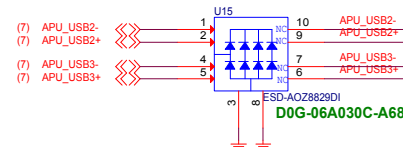
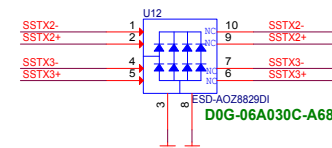
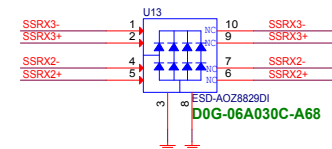
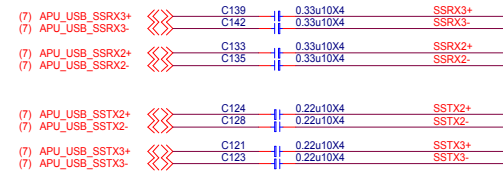
1~5"



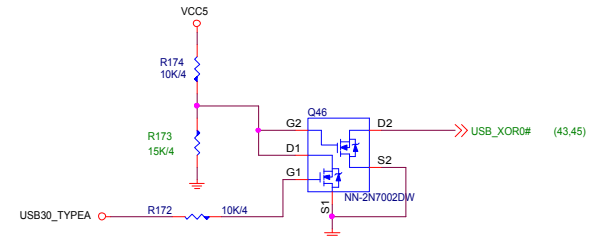
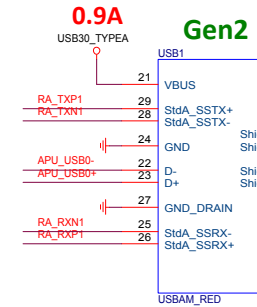
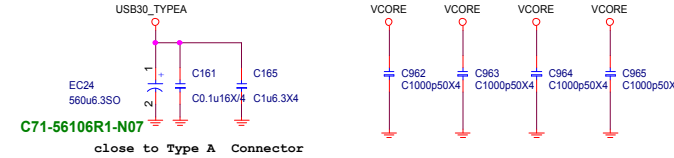
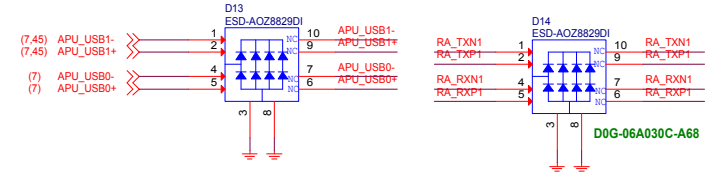
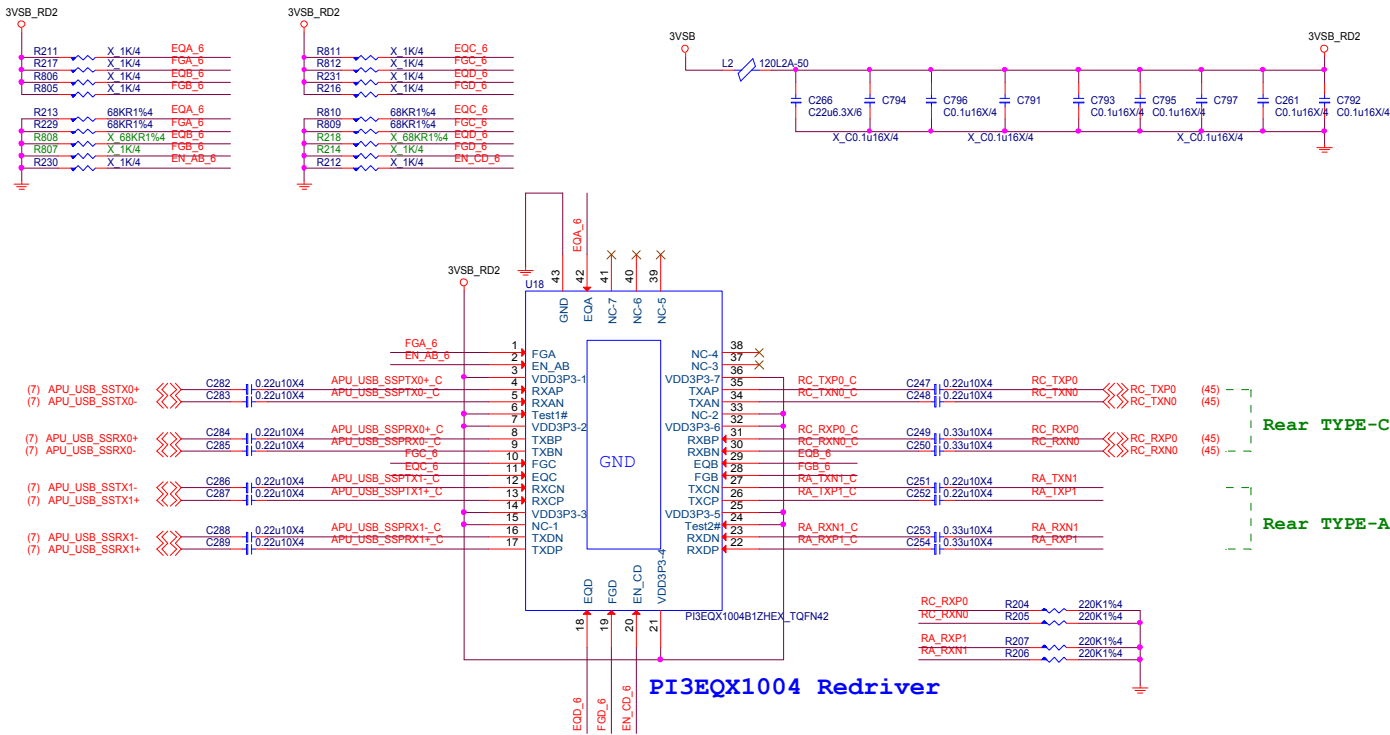
Rear LAN Type-A



HDMI USB3.1 Gen1 Type-A



USB3.1 Gen2 Redriver + Type-A



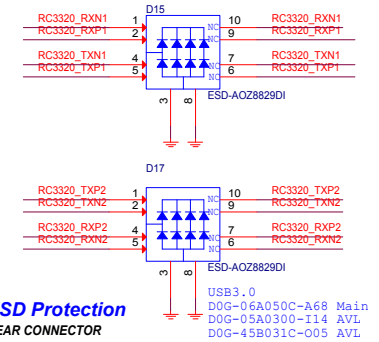
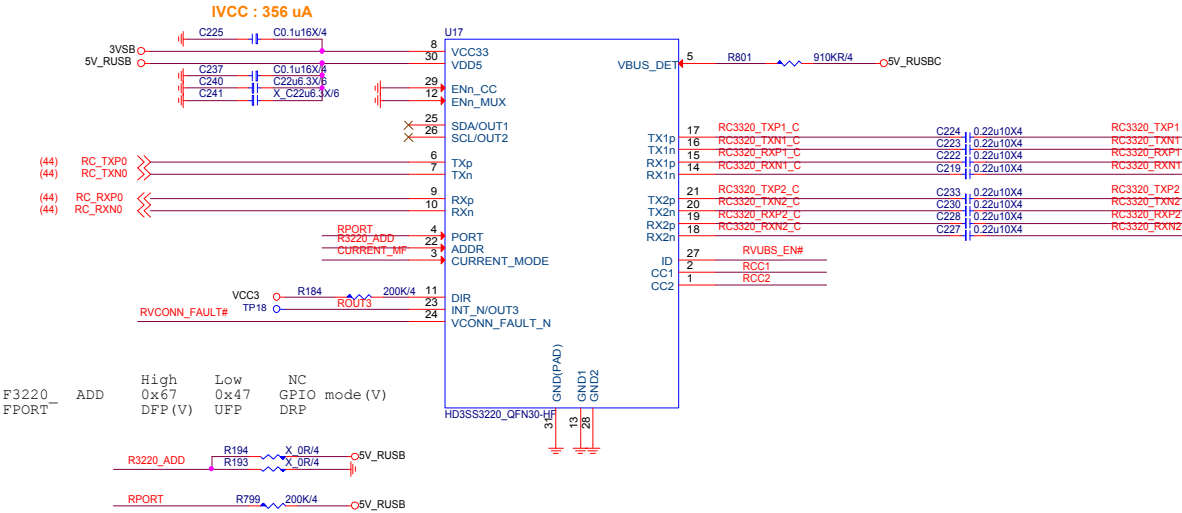
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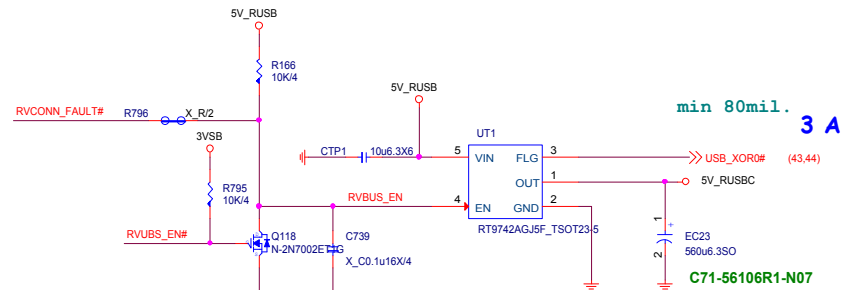
Size	Document Description	Rev
Custom	Rear USB3.1 Type A / redrive	2.2
Date: Thursday, July 16, 2020		Sheet 44 of 75

USB3.1 Gen2 Type-C

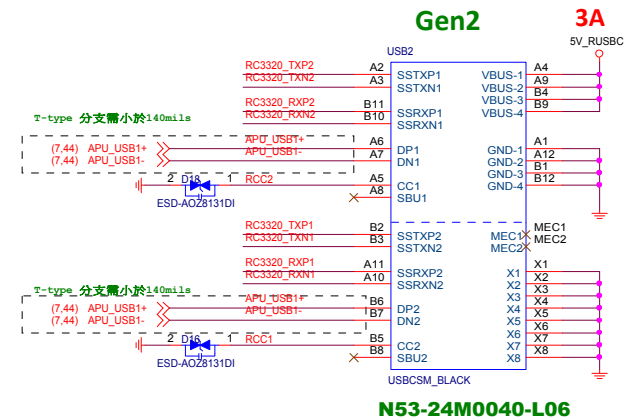
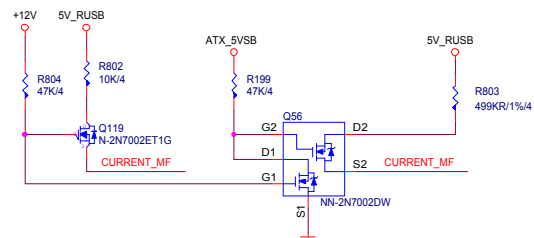
USB Type-C MUX with Configuration Channel (CC)



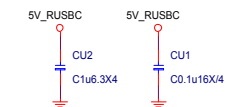
VBUS EN



Current Mode

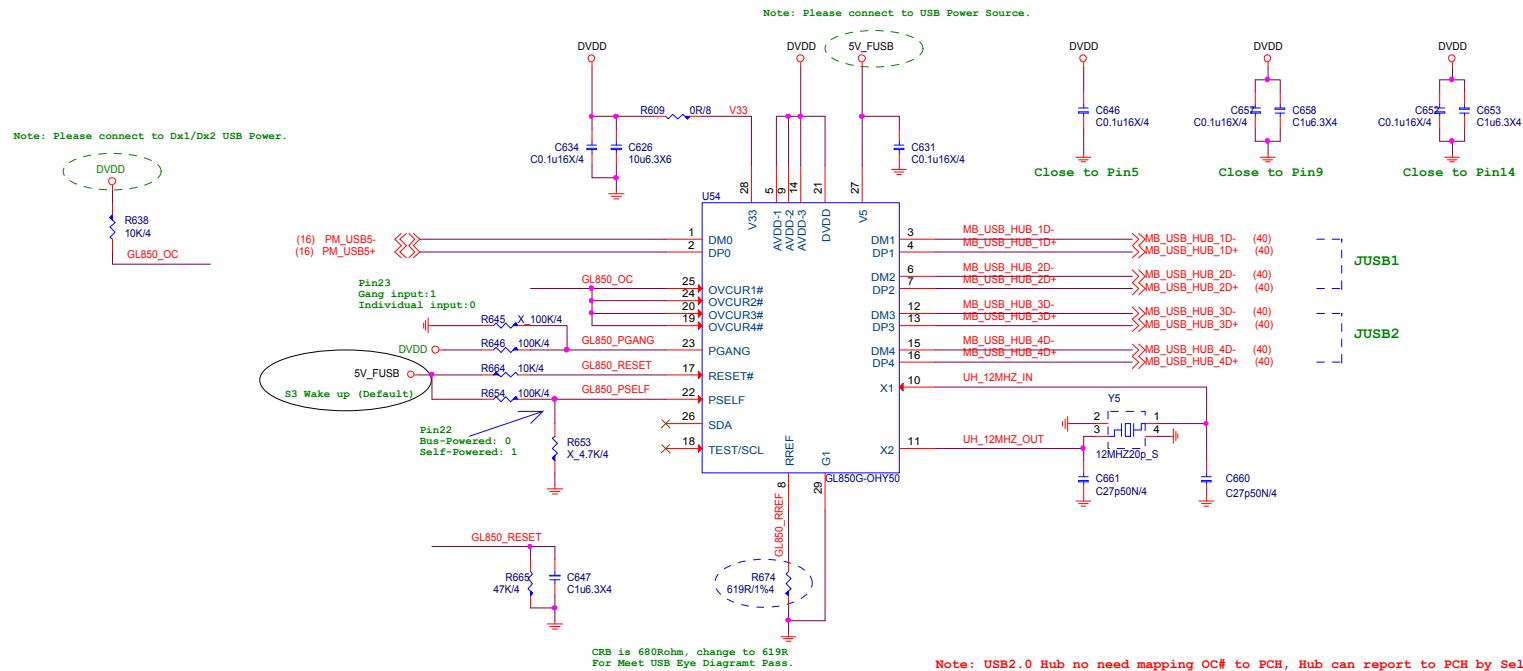


close to Type C Connector



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Size	Document Description		Rev
Custom	Rear USB3.1 Type C / MUX		2.2
Date: Thursday, July 16, 2020		Sheet 45 of 75	

5V_FUSB



Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.



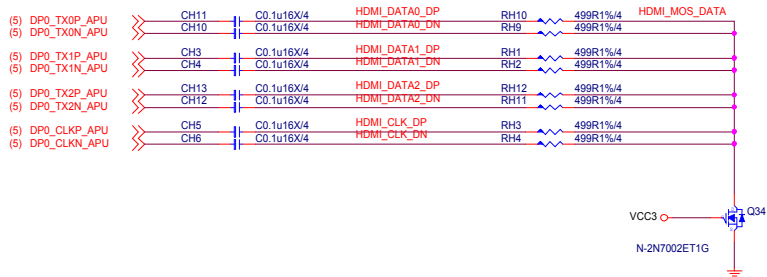
MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description GL850G	Rev 2.2
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HDMI CONNECTOR

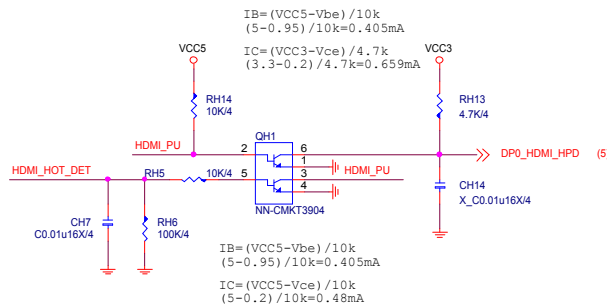
For HDMI 1.4



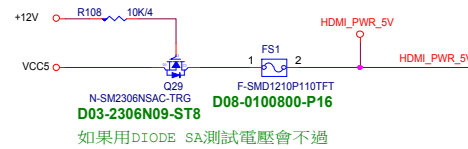
刪除RH6/RH12/RH15/RH16
For 增加VCC5寬度

For EMI

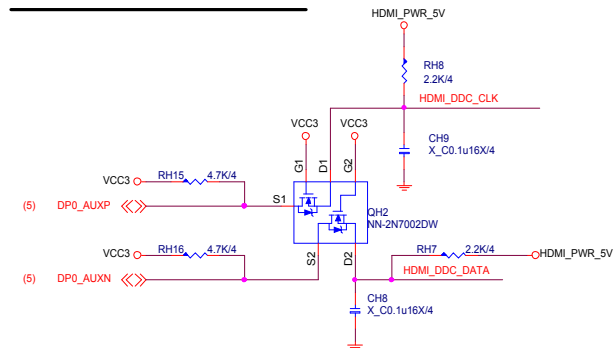
HPD Circuit



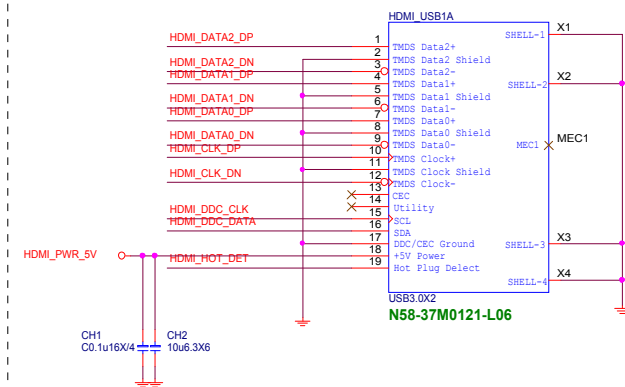
Connector Power



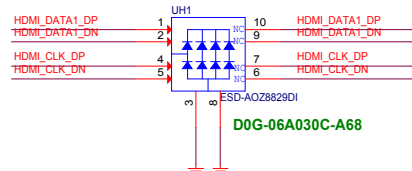
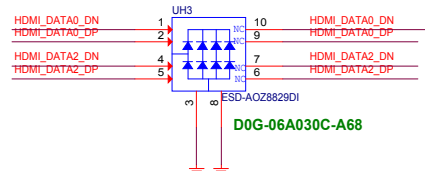
AUX Level Shifter



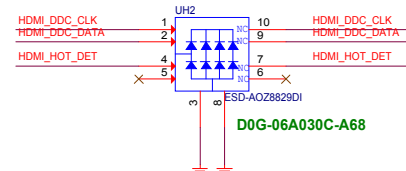
Connector



For EMI



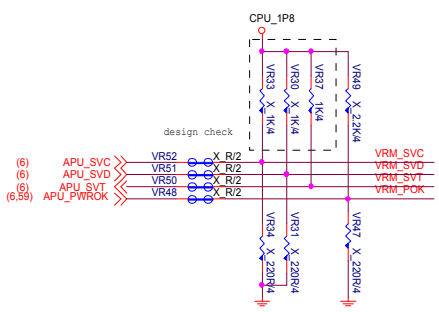
注意:耐壓5v零件



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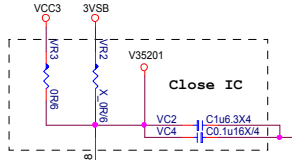
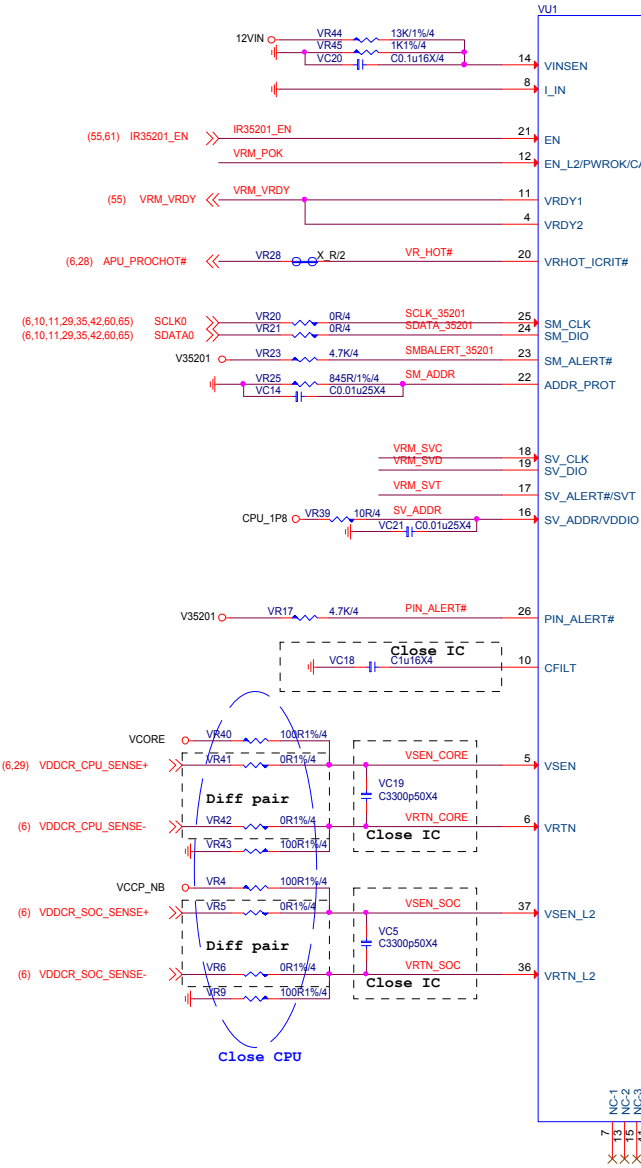
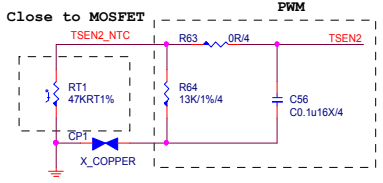
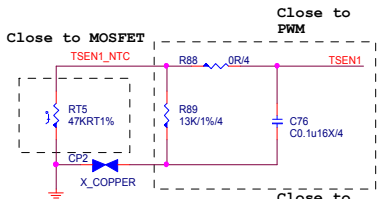
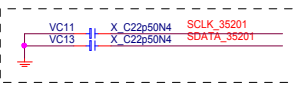
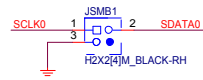
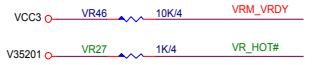
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Size	Document Description	Rev
Custom	HDMI	2.2
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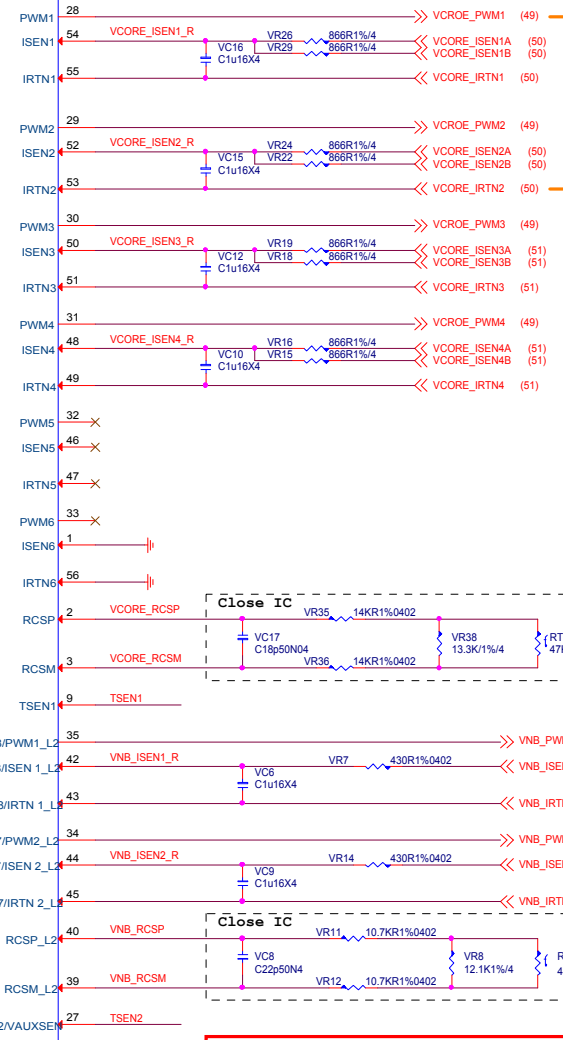


Note:VID Override Circuit

BOOT VOLTAGE		Pre_PWROK Metal VID
SVC	SVD	
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8



燒錄打點:IC正面上橋+金色點



VCORE: ICCMax 140A
LL: 1.3mohm
OCP: 192A

SOC: ICCMax 75A
LL: 2.1ohm
OCP: 90A

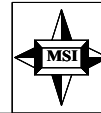
Phase 1 close to CPU power pin.

RT close to Choke

RT close to Choke

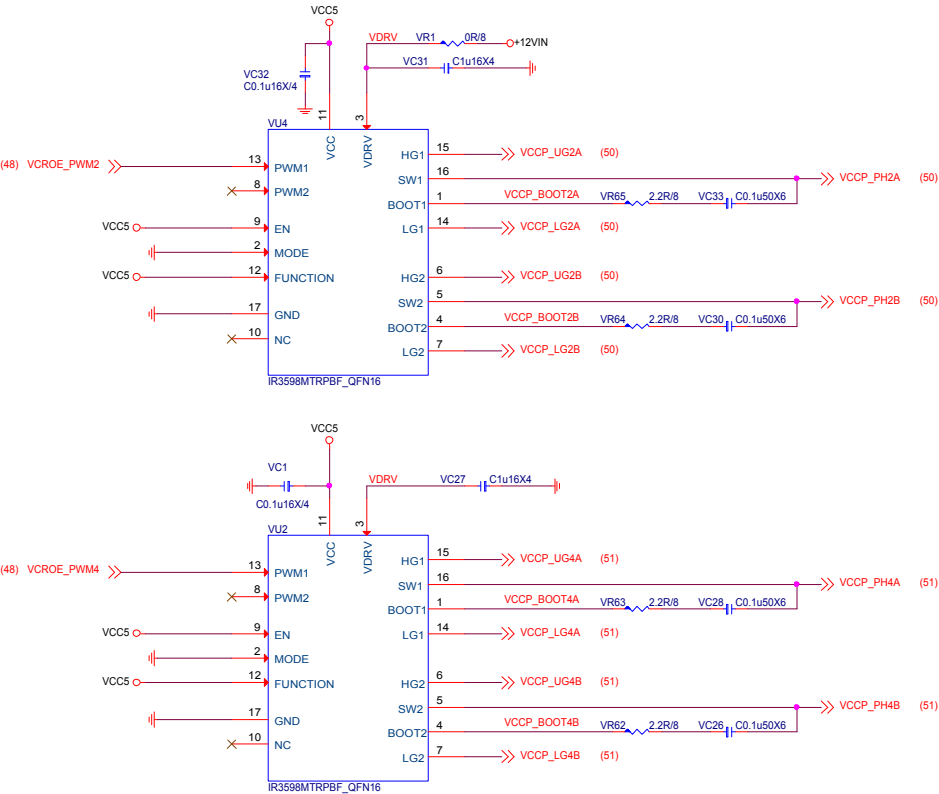
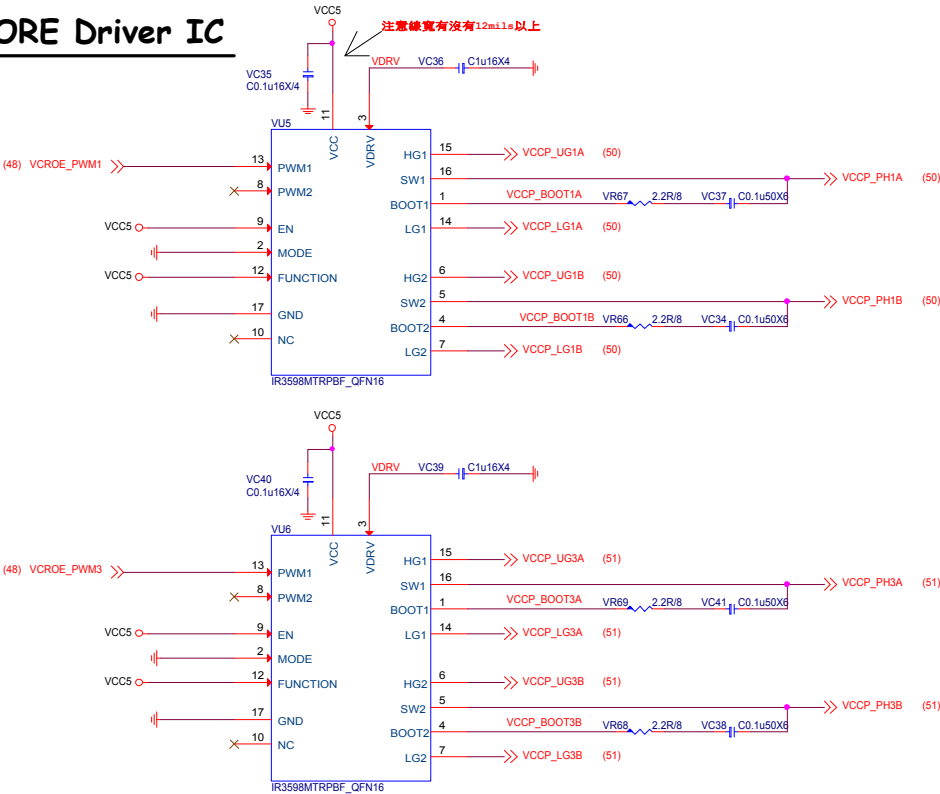
0x26: RH=18K, RL=13K

Default		VR53	VR54	VC20	VR58	VR57	VR59	VR60
Temp	6.49k	10k	100p	X	0R	X	0R	0R
VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X	X



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Size	Document Description	Rev	
Custom	CPU Power IR35201 8+2	2.2	
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CPU_CORE Driver IC



CPU_SOC Driver IC

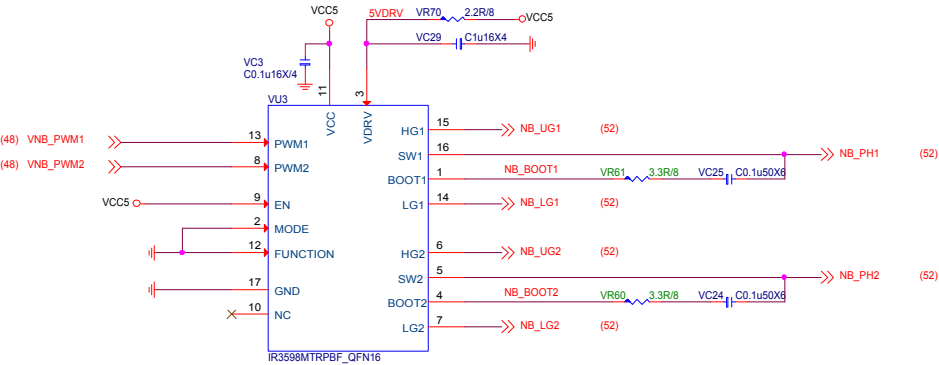


Table for IR3598

Function	Mode	PWM Mode	Phase Mode
0	1	IR ATL	Dual
1	1	IR ATL	Doubler
0	0	Tri-State	Dual
1	0	Tri-State	Doubler

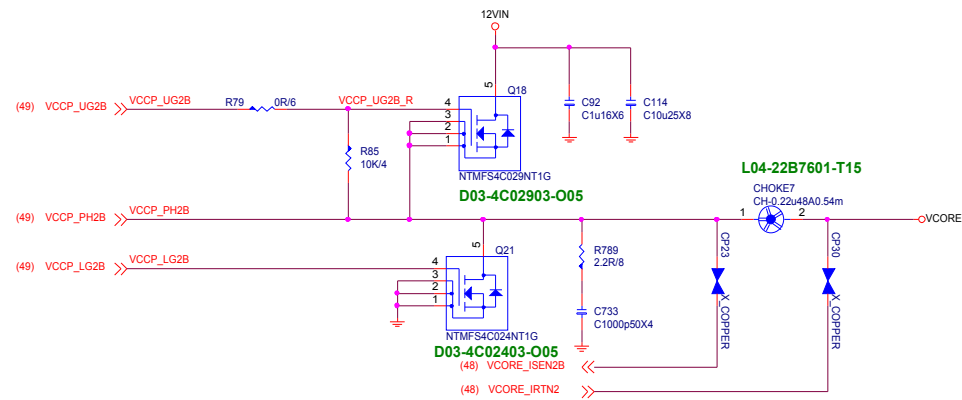
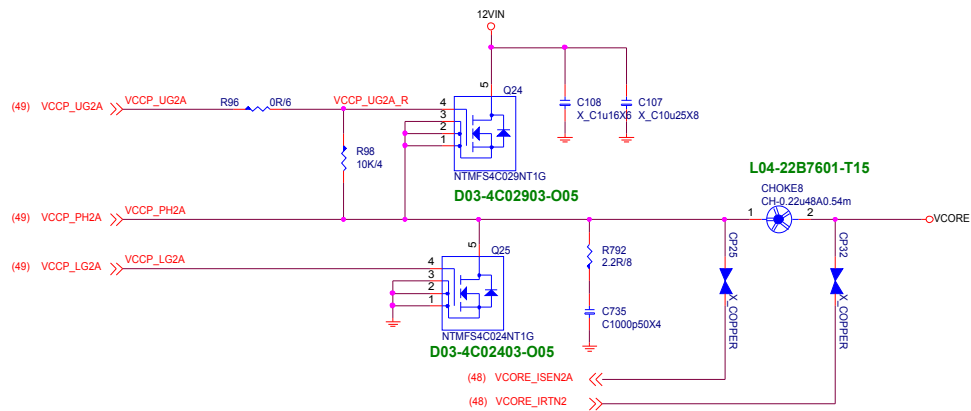
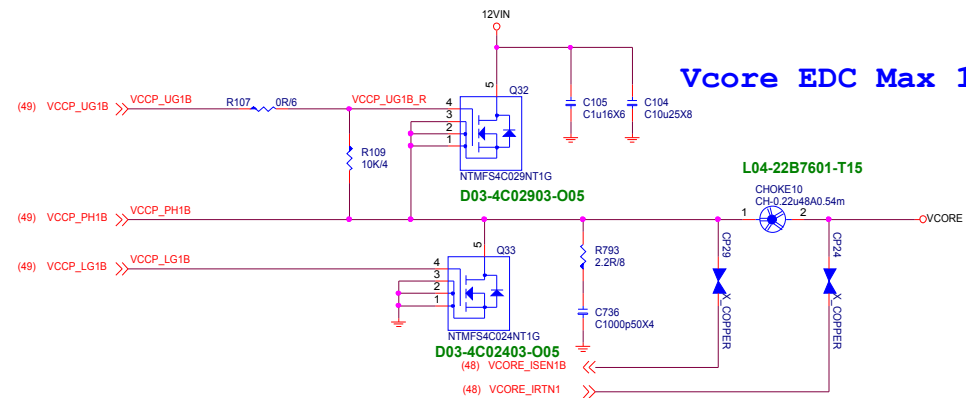
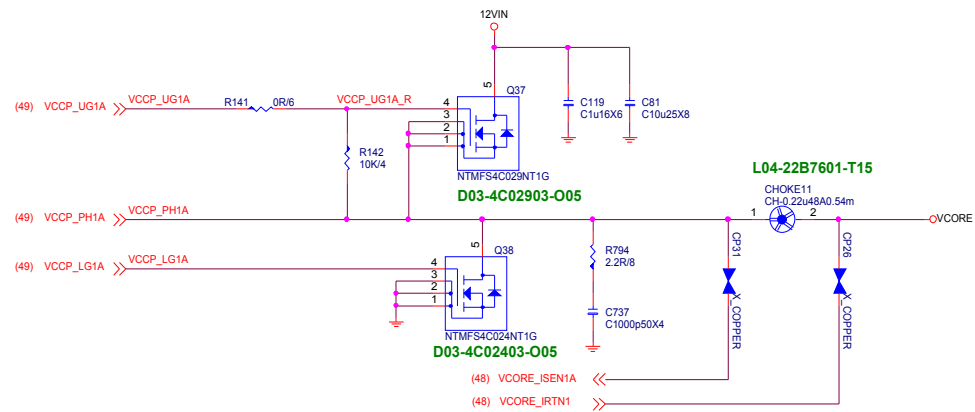
0	0	Tri-State	Dual	SOC
1	0	Tri-State	Doubler	Vcore



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Size	Document Description	Rev
Custom	CPU Power Driver IC IR3598	2.2
Date:	Thursday, July 16, 2020	Sheet 49 of 75



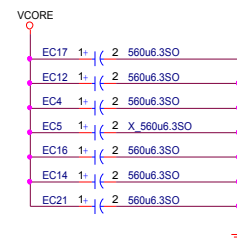
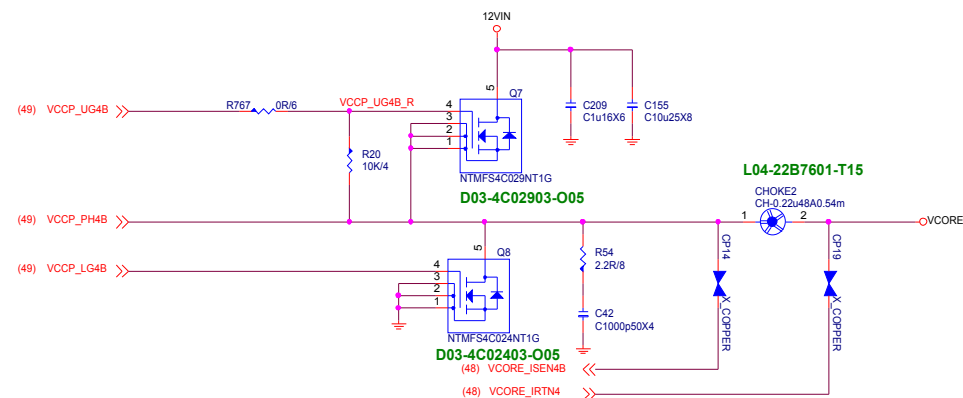
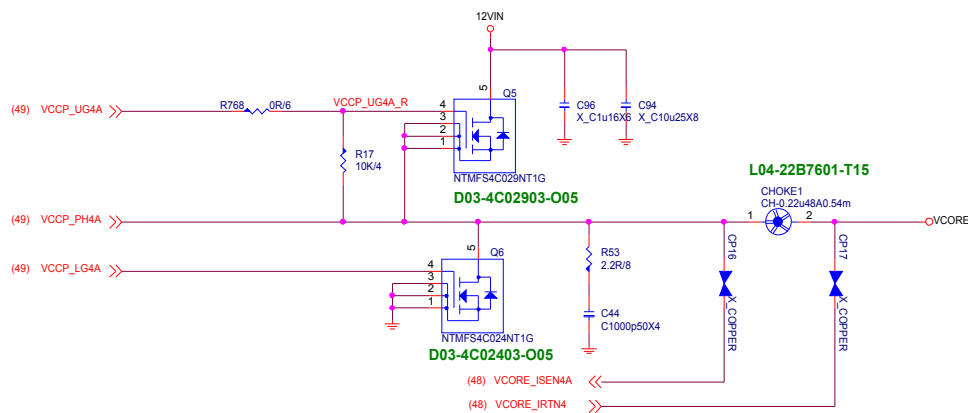
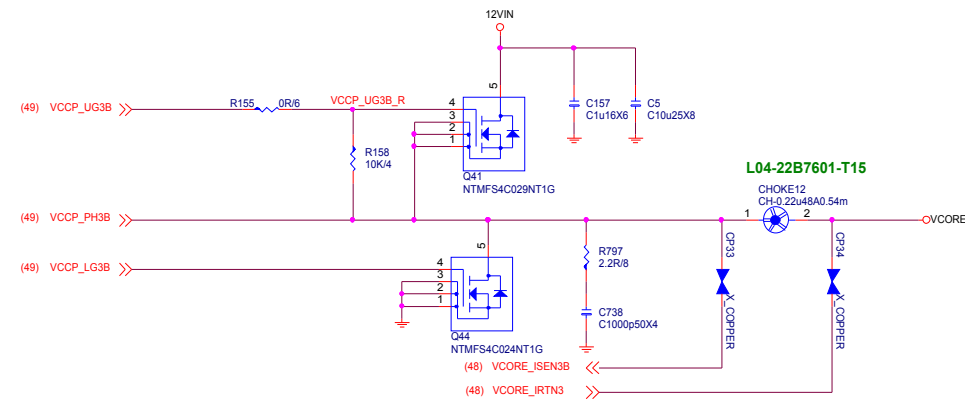
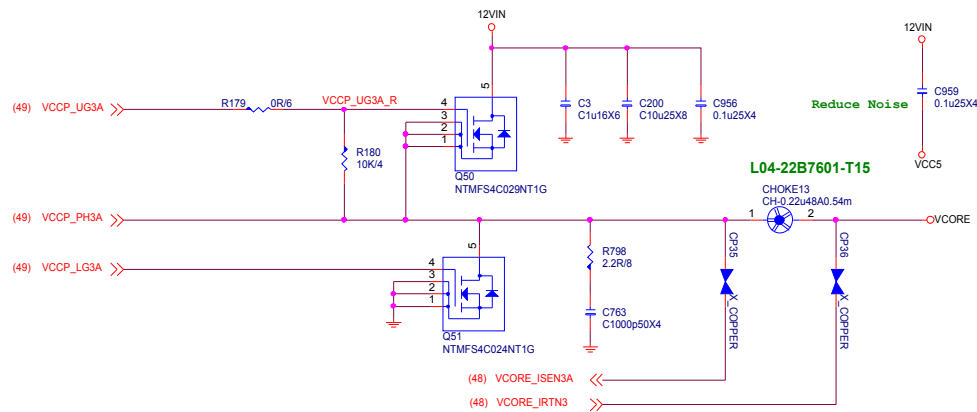
Vcore EDC Max 140A

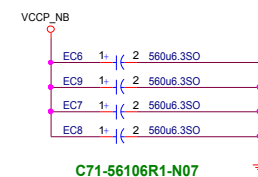
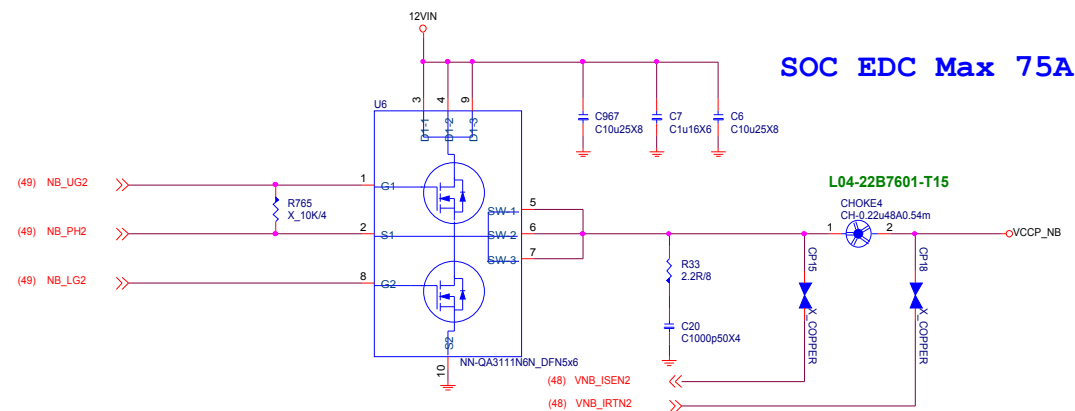
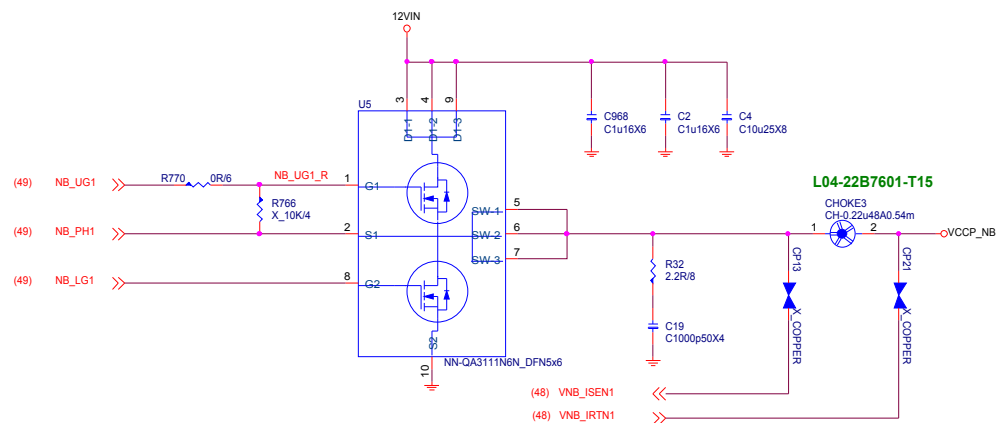


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Size	Document Description	Rev
Custom	CPU Power Vcore Phase 1-6	2.2
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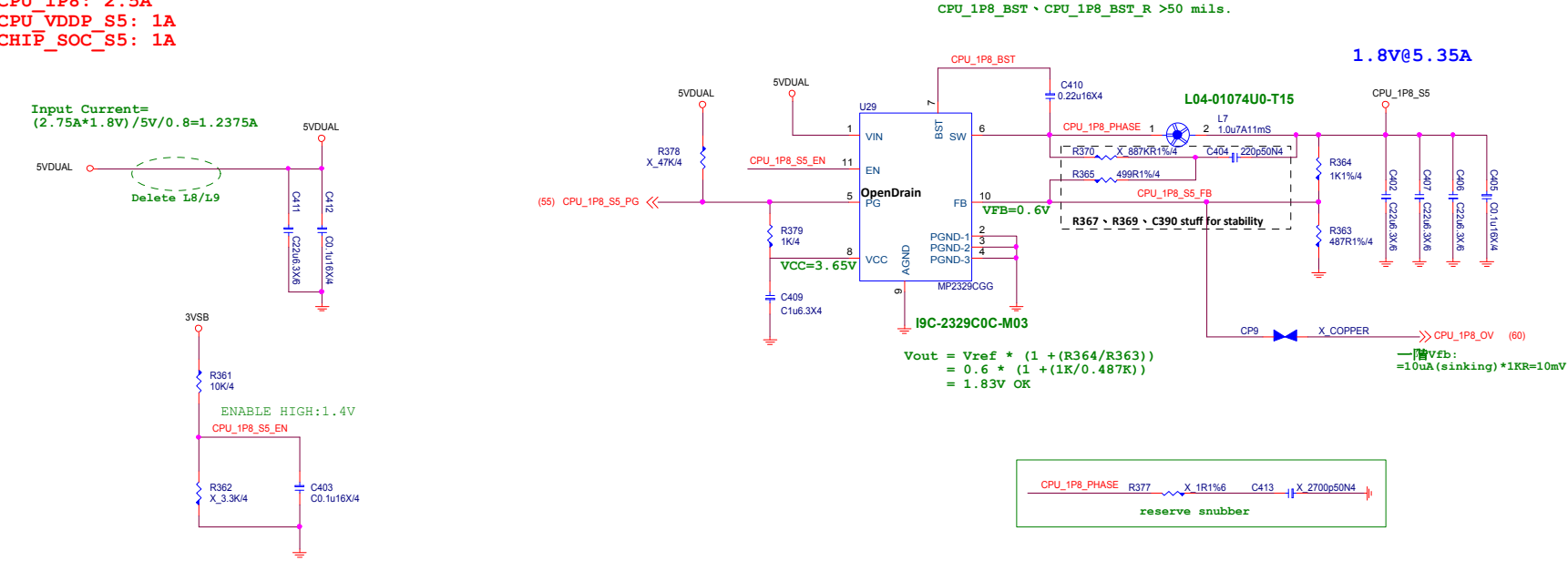
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Size	Document Description	Rev
Custom	CPU Power NB Phase 1-2	2.2
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CPU 1P8V S5

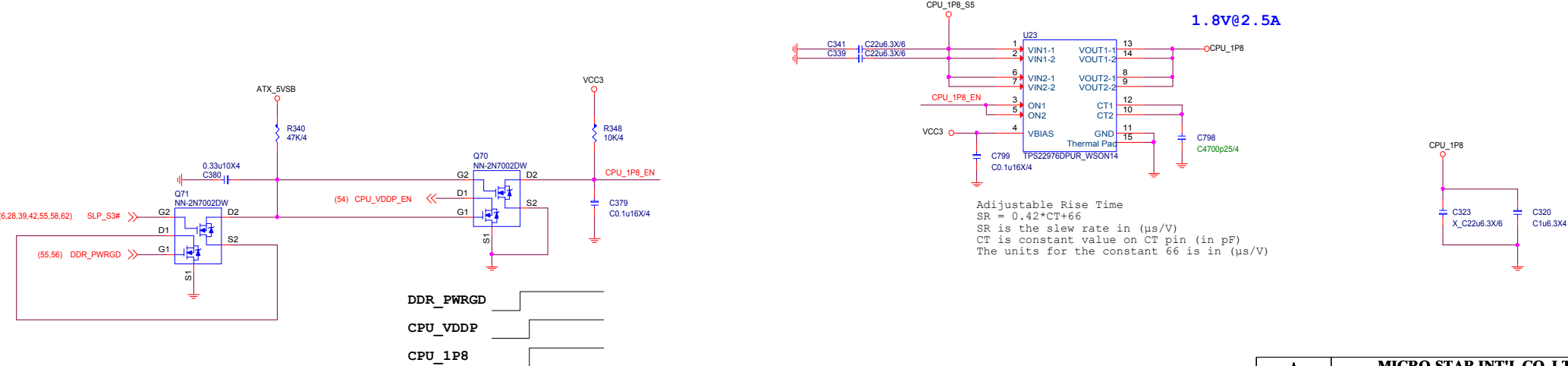
CPU: VDD 18 S5@0.5A
CPU: VDDIO Audio@0.25A
CHIP: VDD_I8_S5@0.1A

CPU_1P8: 2.5A
CPU_VDDP_S5: 1A
CHIP_SOC_S5: 1A



CPU 1P8V

CPU: VDD 18@2A
CHIP: VDD_18@0.5A



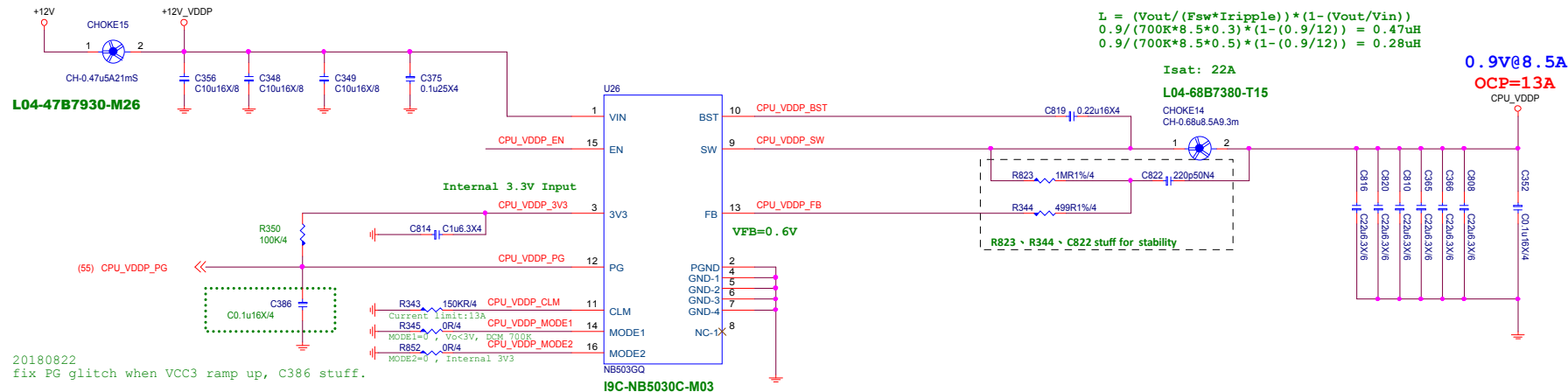
MICRO-STAR INT'L CO.,LTD

MS-7C37

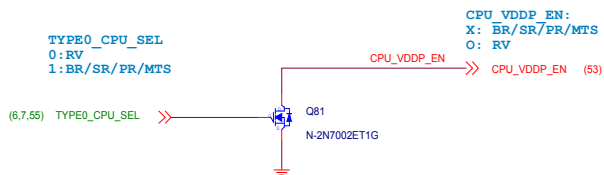
Size	Document Description	Rev
Custom	CPU Power 1.8_S0 / S5	2.2
Date:	Thursday, July 16, 2020	Sheet 53 of 75







CPU: VDDP@8.5A

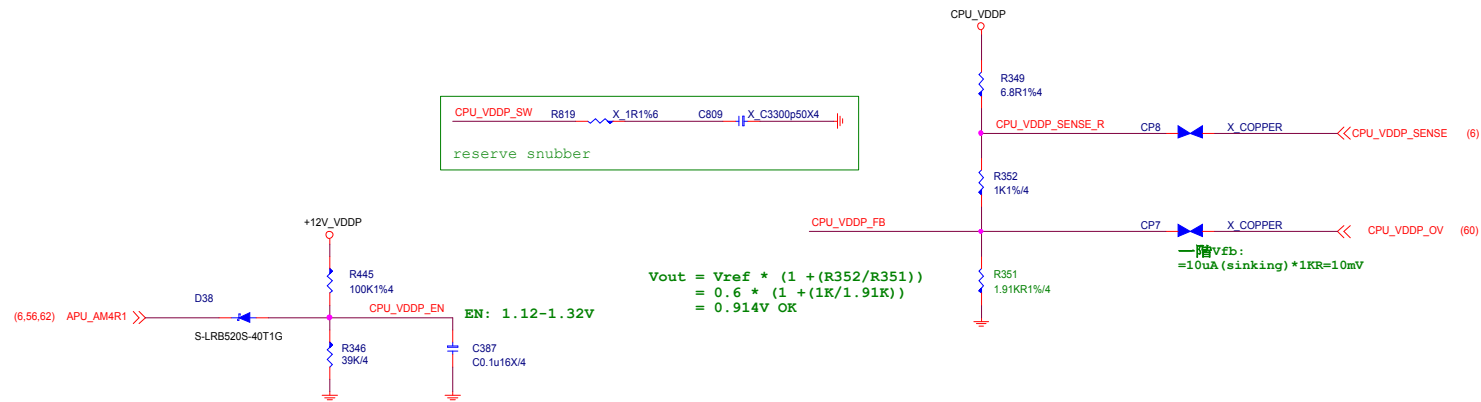
```
Input Current = (8.5A*0.9V)/12V/0.8 = 0.8A
Choke Isat = 8A
Irms=Iout*SQRT( (Vo/Vi) *(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms = 5 A
```



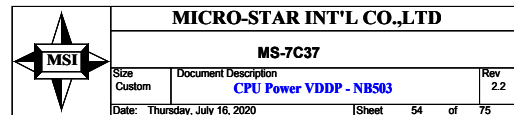
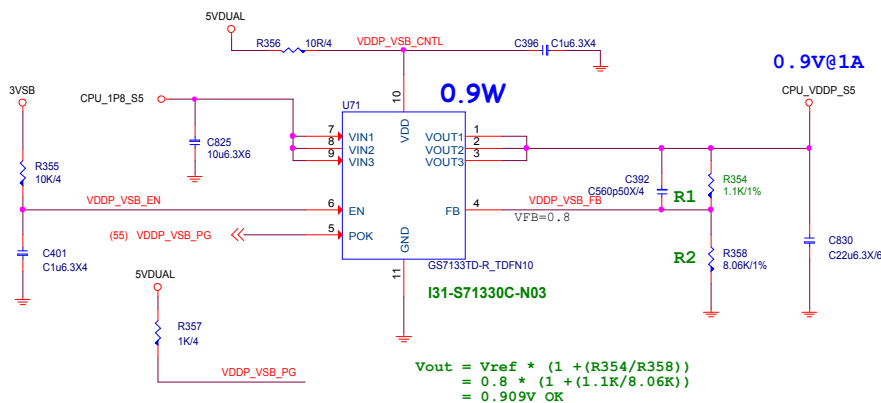
No support BR SPEC



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1		SPEC not Support
NA		0		0
SR	2	1		CPU VDDP NOT SUPPORT TYPE2
RV/ZP	3	0		1
MTS	4	1		CPU VDDP NOT SUPPORT TYPE4

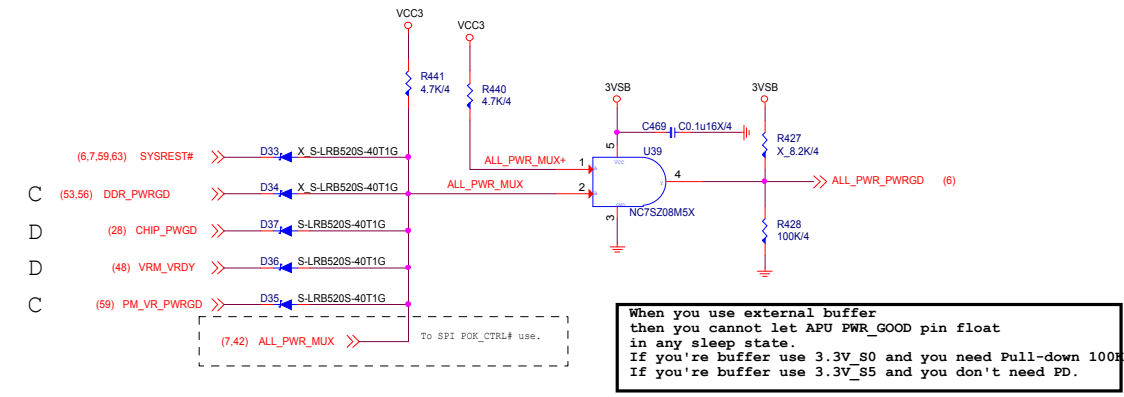


CPU: VDDP S5@1A

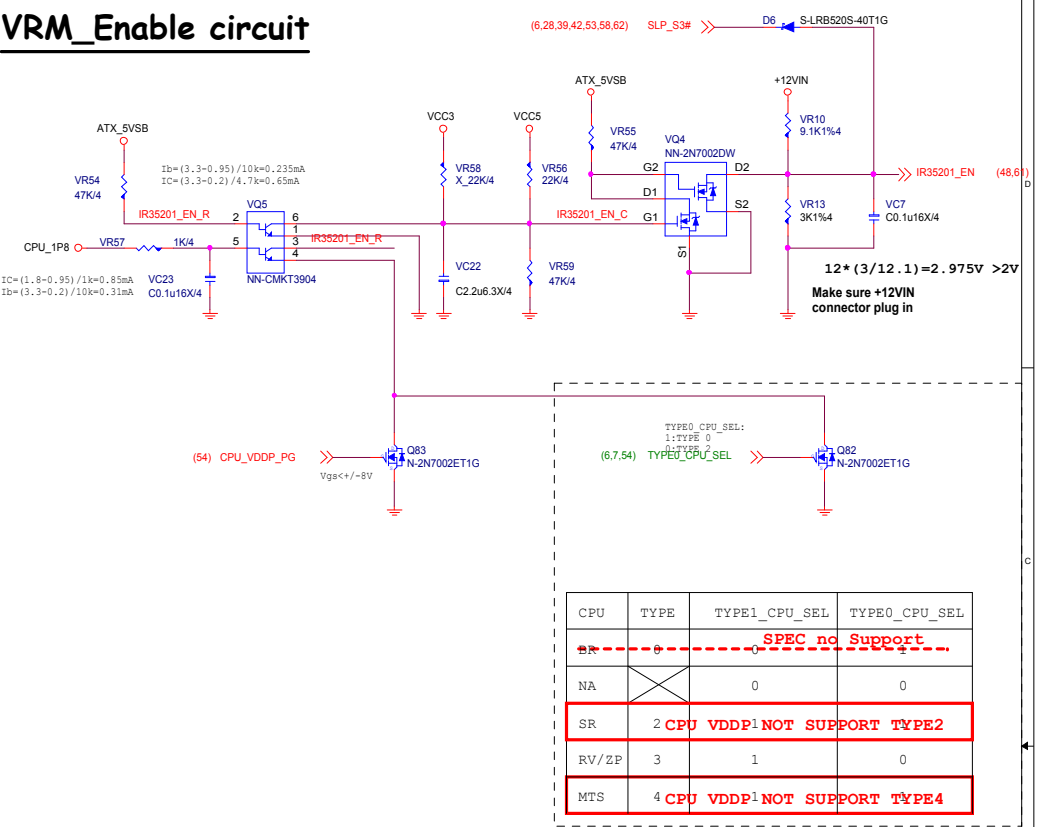


ALL POWER GOOD MUX

S0 PG

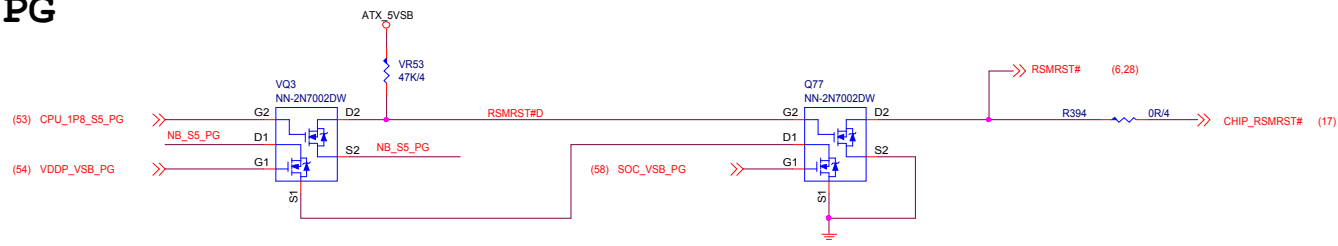


VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
NA		0	0
SR	2 CPU VDDP1 NOT SUPPORT TYPE2		
RV/ZP	3	1	0
MTS	4 CPU VDDP1 NOT SUPPORT TYPE4		

S5 PG



VCC_DDR

15.5A For CPU
9.5A For 4DIMM
1.2A For DDR VTT

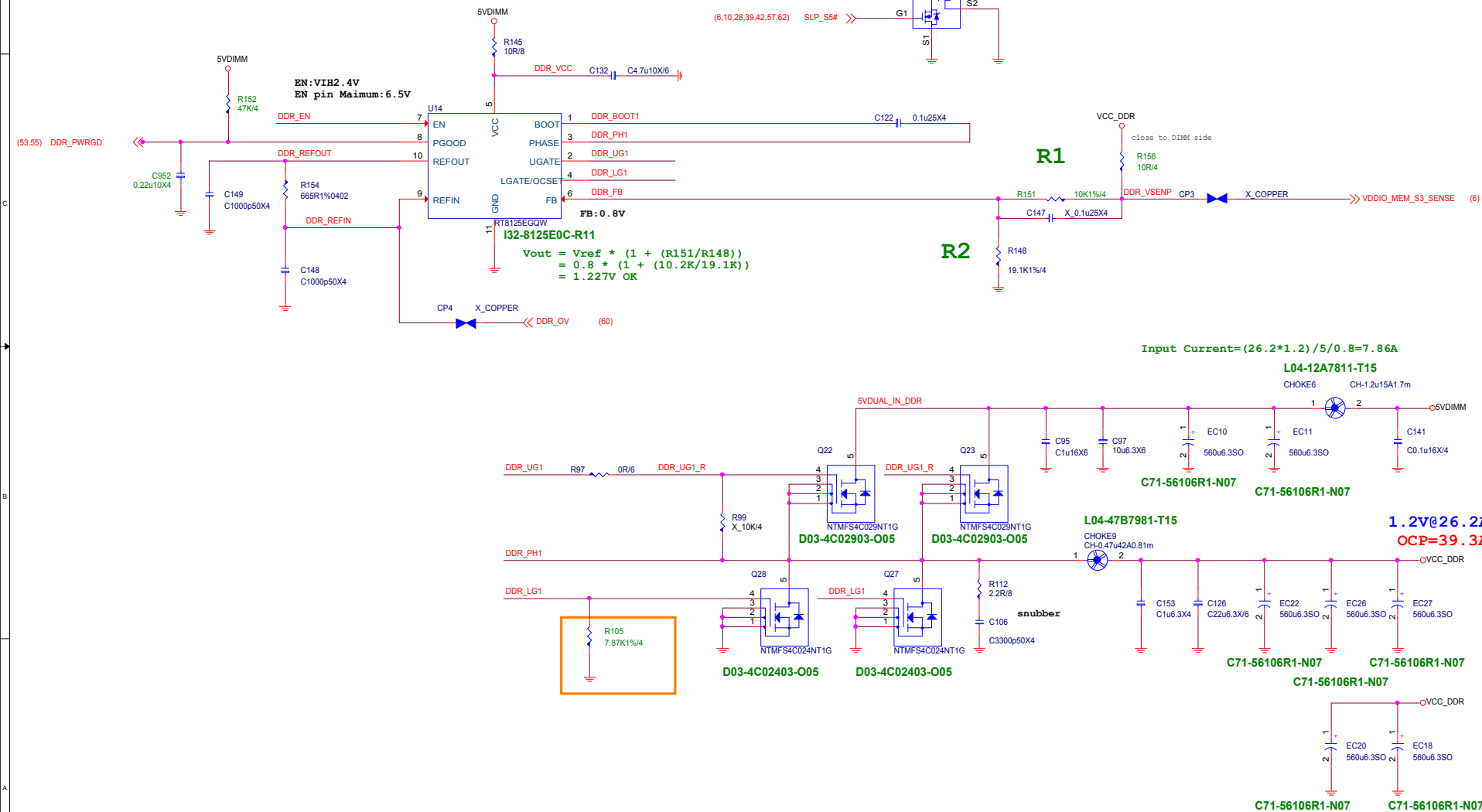
OCP = 39.3A; Choke Isat=42A

$R_{ocset} = 1.5 * I_{max} * R_{dson(LOW)} / I_{ocset}$
 $R_{649} = 1.5 * 26.2 * 2m\Omega / 10\mu A$
 $R_{649} = 7.86K$

$R_{dson(LOW\ Side)} 5V$
 $D03-4C02403-005: 3.3 \sim 4m\Omega$
 $4m\Omega / 2pcs = 2m\Omega$

$$R_{ocset} = \frac{I_{VALLEY} \times R_{LGS(ON)}}{I_{ocset}}$$

Current Sensing				
Iocset			9	10
			11	12



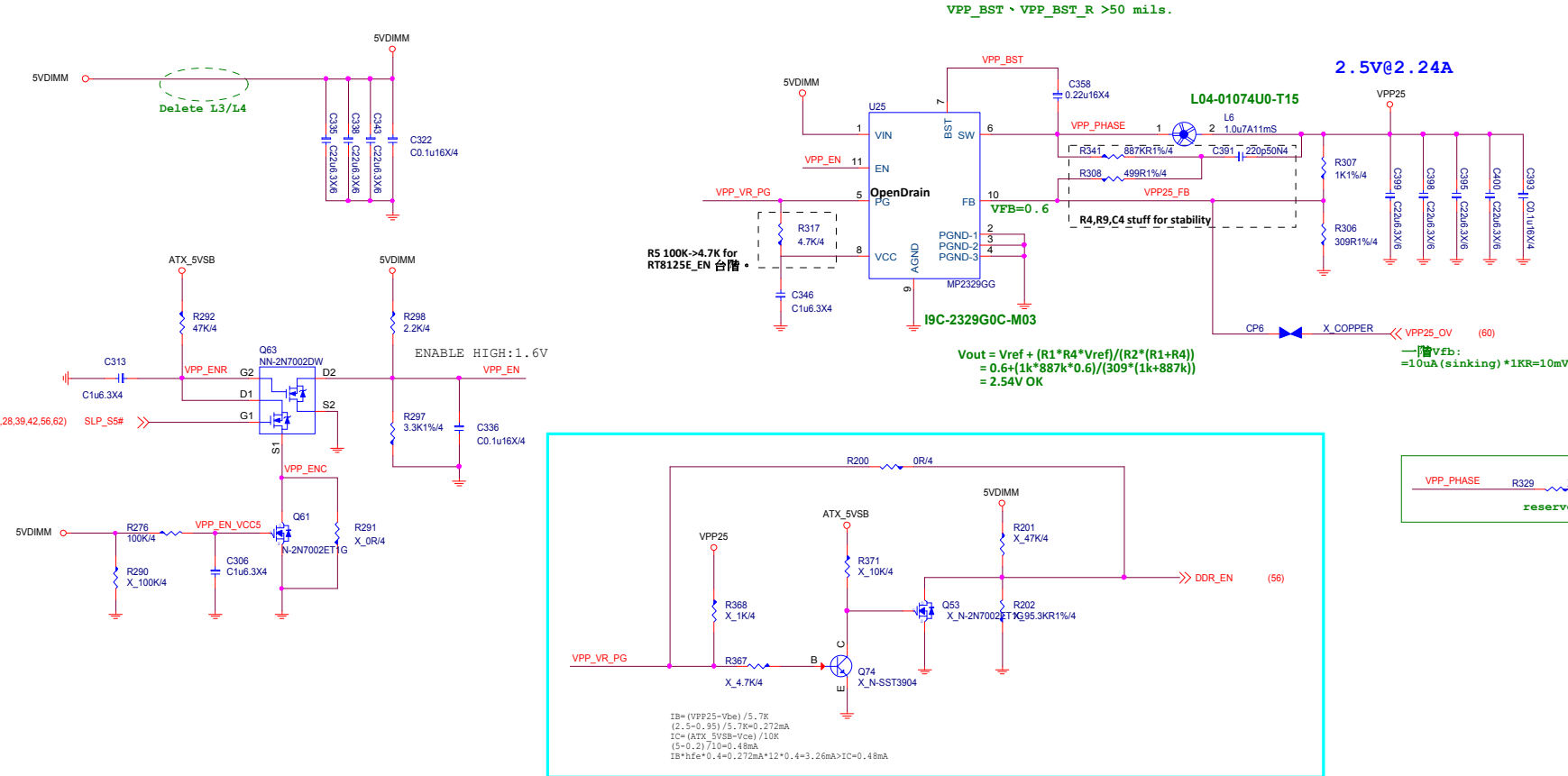
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Size	Document Description	Rev
Custom	DDR Power - 812SE	2.2
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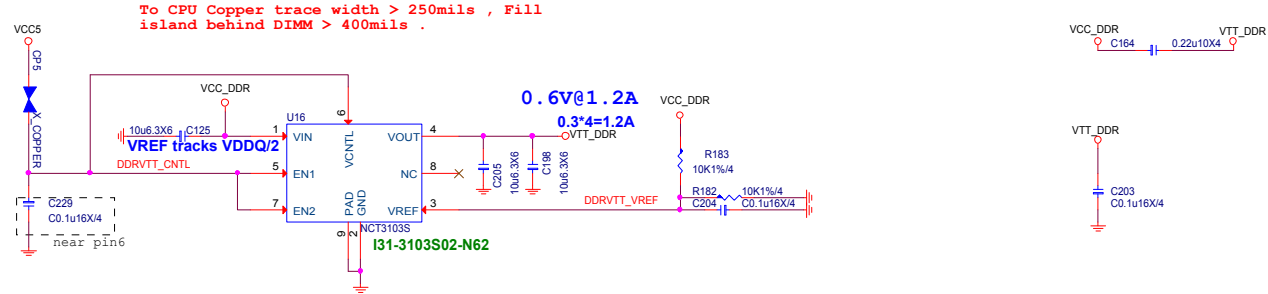
VPP25

2.5V@2.24A



VTT DDR

0.6V@1.2A



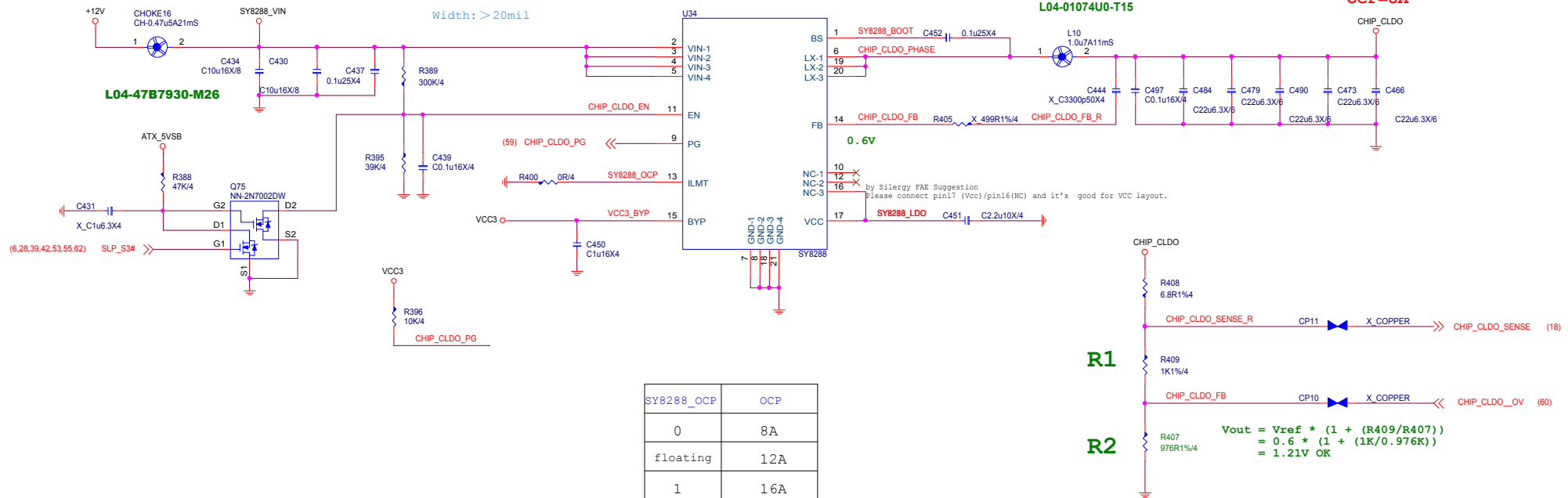
CHIP CLDO

CHIP: VDD_CLDO@5A

Input Current= (5.5A*1.05V)/12V/0.8=0.625A

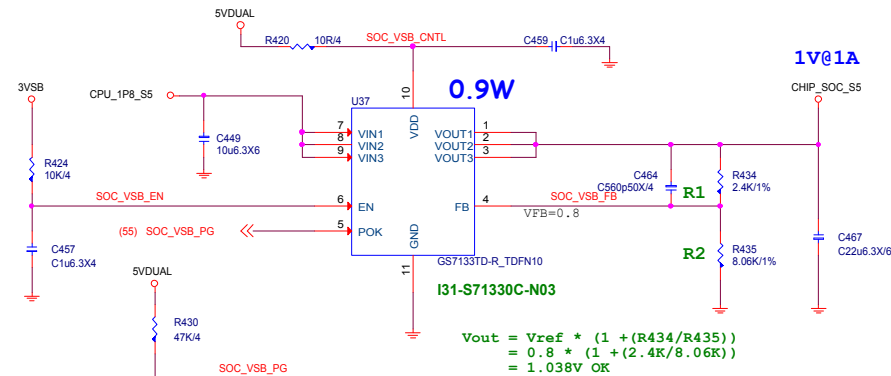
1.2V@5A

OCP=8A



CHIP SOC S5

CHIP: VDDCR_SOC_S5@1A

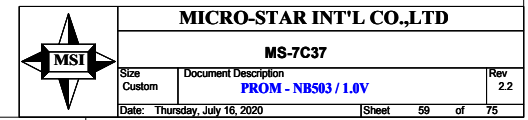
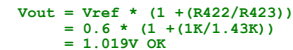


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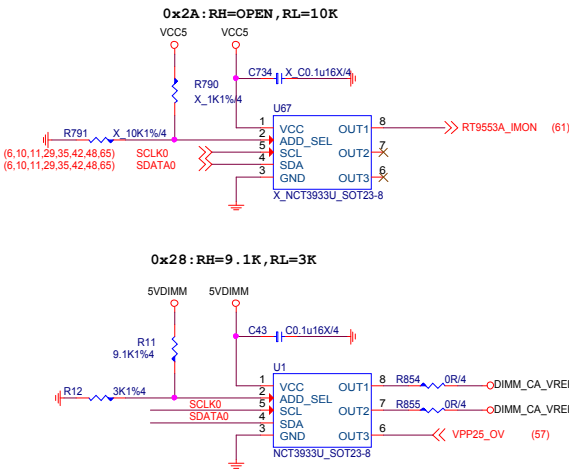
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Size	Document Description	Rev
Custom	PROM - SY8288RAC / 1.05V	2.2
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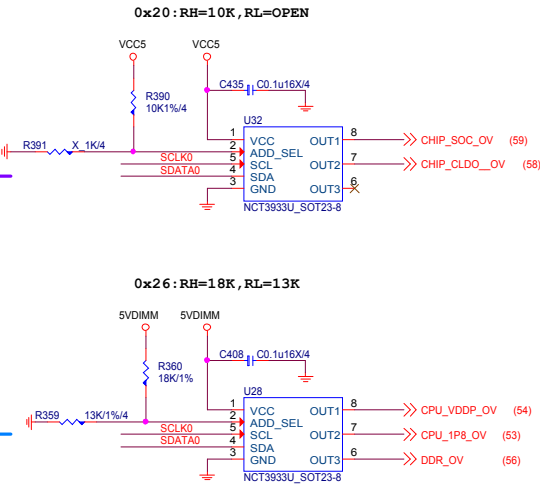
CHIP: VDDCR_SOC@9A

$$\begin{aligned} L &= (V_{out}/(F_{sw} \cdot I_{ripple})) \cdot (1 - (V_{out}/V_{in})) \\ 1/(700K \cdot 12 \cdot 0.3) \cdot (1 - (1/12)) &= 0.432\mu H \\ 1/(700K \cdot 12 \cdot 0.5) \cdot (1 - (1/12)) &= 0.218\mu H \end{aligned}$$


Over Voltage Control IC



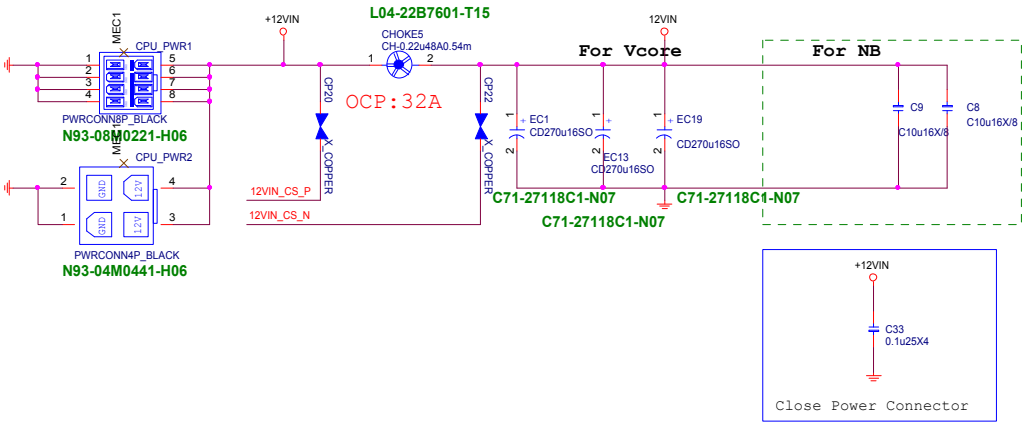
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



UPI VOLTAGE CONSOLE

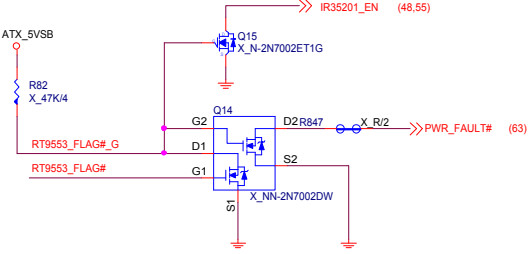
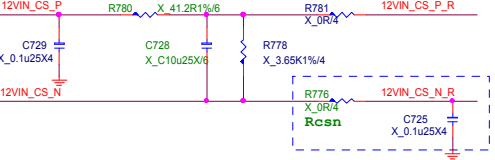
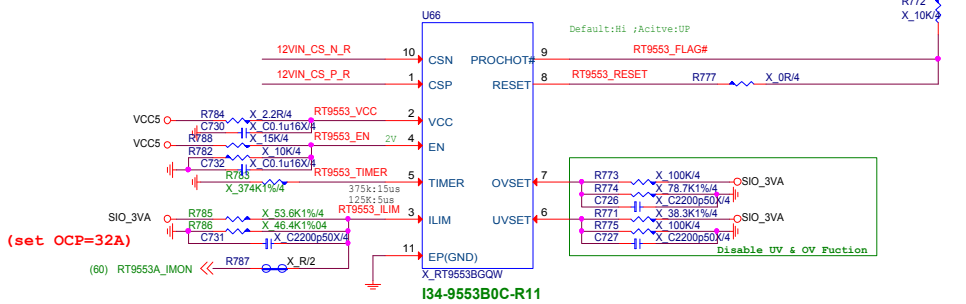
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

CPU POWER CONNECTOR



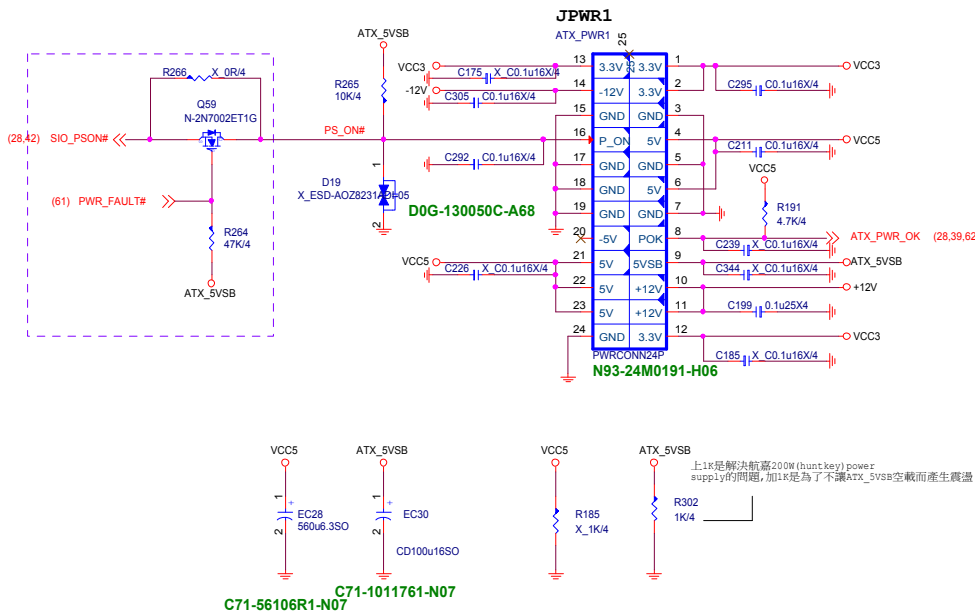
RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.

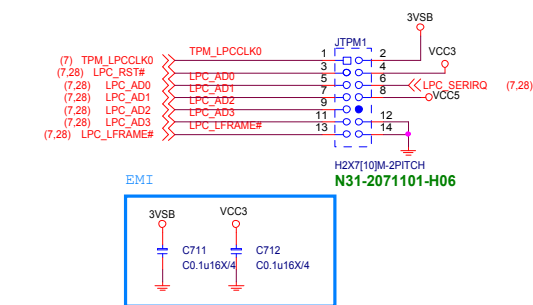


Vcore		SOC	
D=Vout/Vin		D=Vout/Vin	
Vin = 12	> input voltage	Vin = 12	> input voltage
Vout = 2	> output Vcore	Vout = 1.55	> output Vcore
D = 0.166667		D = 0.129167	
Io = Icore(max)*0.8		Io = Icore(max)*0.8	
I core(max) = 200	> Vcore current	I core(max) = 75	> Vcore current
I avg. = 160	A	I avg. = 60	A
I ripple={ Io*√ D*√ (1-D) } / Phase		I ripple={ Io*√ D*√ (1-D) } / Phase	
Phase = 10	phase	Phase = 2	phase
I ripple = 5.962848	A	I ripple = 10.06153	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I ripple(cap) = 4700	m A	I ripple(cap) = 4700	m A
COETEMP = 1		COETEMP = 1	
Input Cap. = 2	pcs.	Input Cap. = 3	pcs.

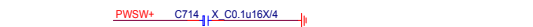
ATX POWER CONNECTOR



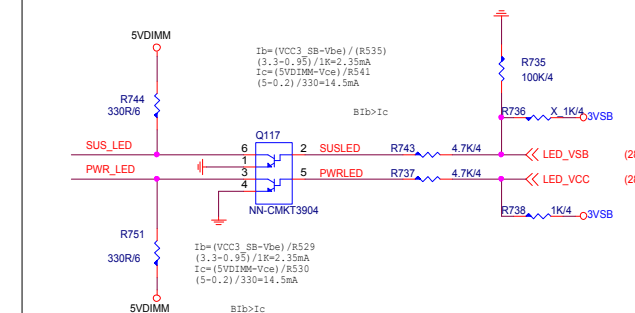
TPM



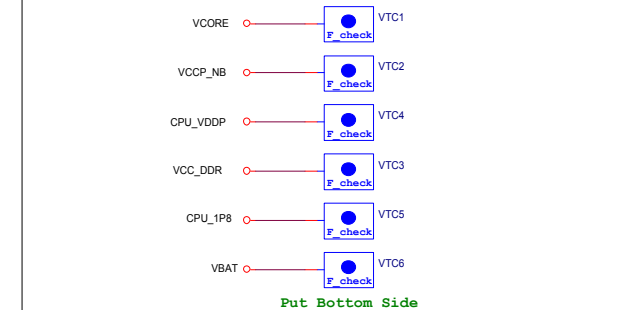
Add for EMI



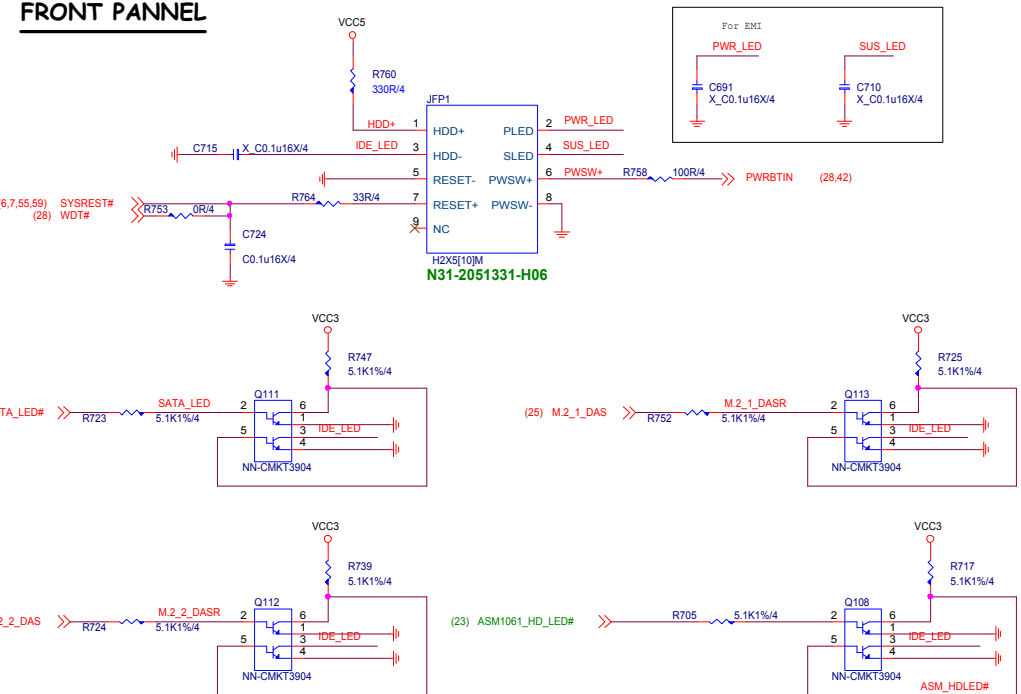
LED (for NCT6797D)



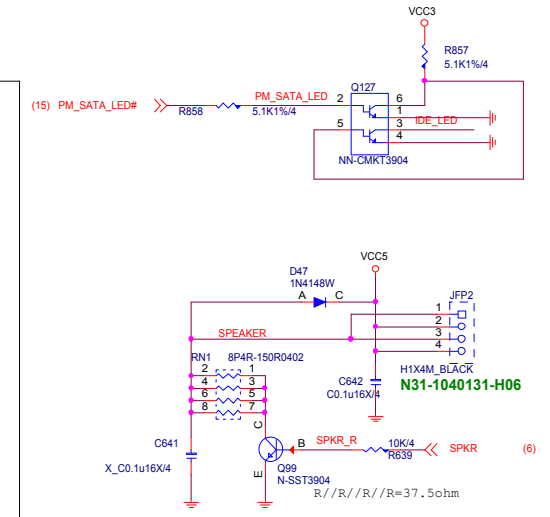
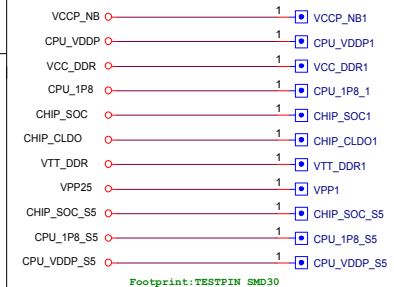
Factory check point



FRONT PANNEL



Voltage Mearsure Point



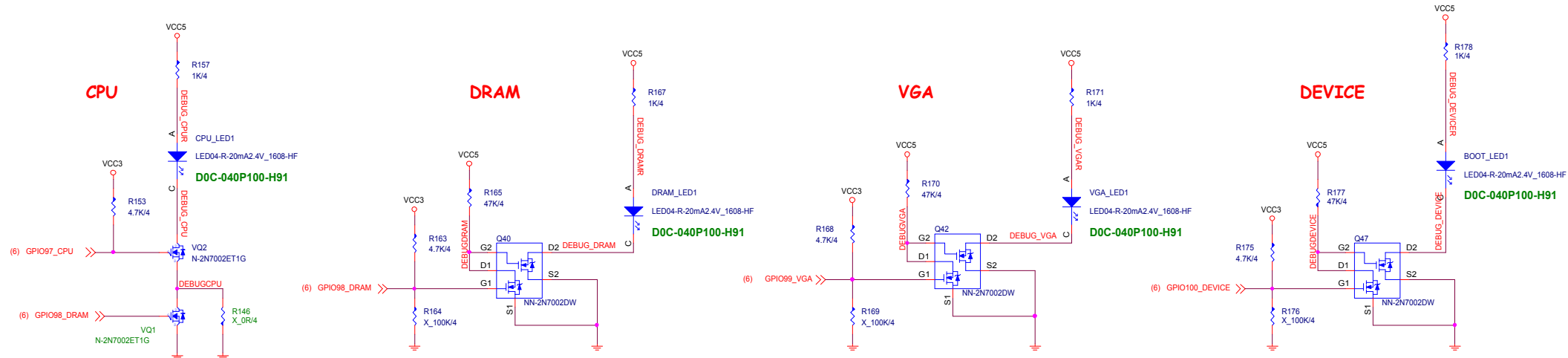
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Size	Document Description	Re
Custom	ATX Power - FrontPanel / EMI	2

2.2

EZ Debug LED



LED亮燈時同時將CPU LED關掉

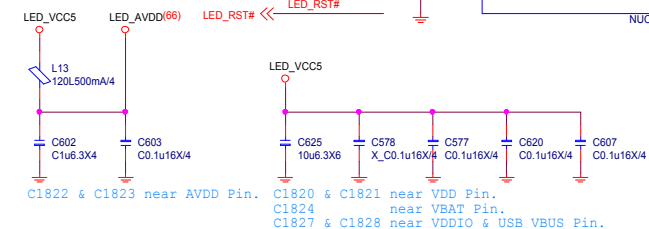
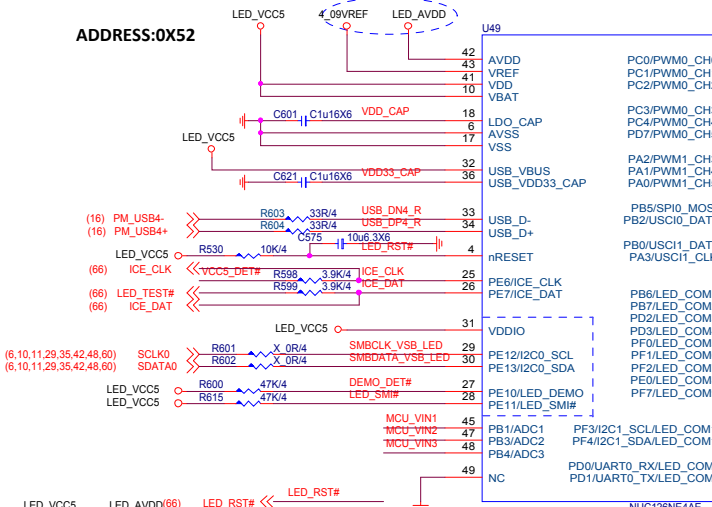
LED GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

AMD AMP Detect LED

48 PIN LED MCU

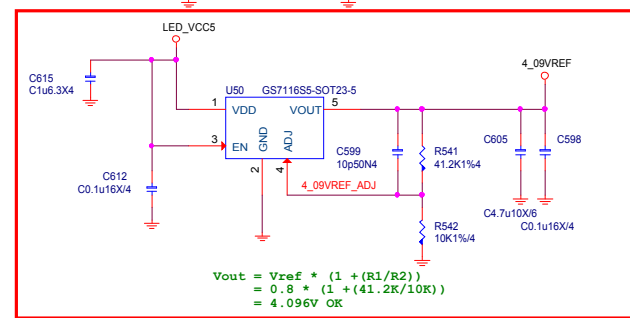
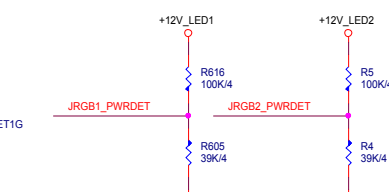
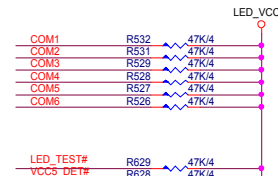
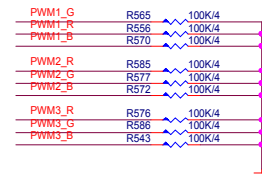
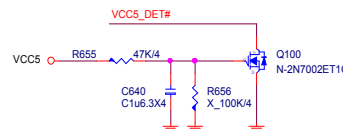
If you use ADC function, need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52

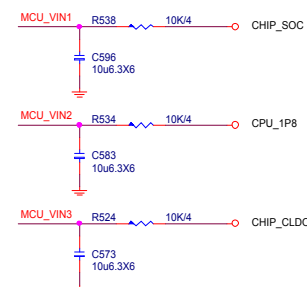


If SPEC has LED demo function without demo button, DEMO_DET# must pull up to LED_VCC5, Q101 need to stuff and control by LED_VCC5_EN. PS. R630 remove, R600 and Q101 need to stuff

PS. COM1 is the first action block, next is COM2, and so on. Pin15,16 can configure to master smbus if spec requirement.

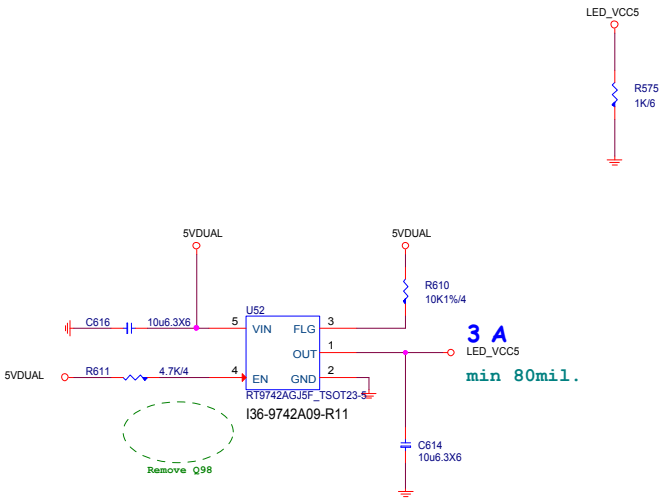


Option Spec For Voltage Monitor Require.



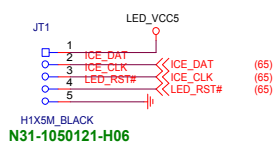
Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

EXTERNAL POWER INPUT



External Power

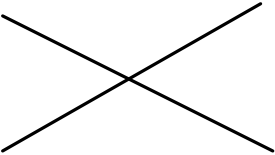
JT1 for FW update



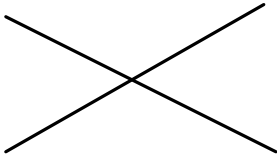
JF1 For Factory Test



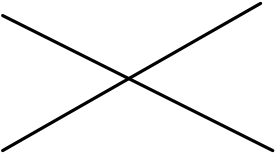
1 PCH HEATSINK LED



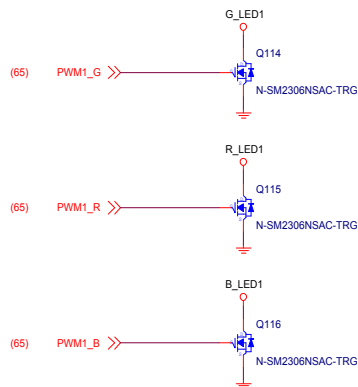
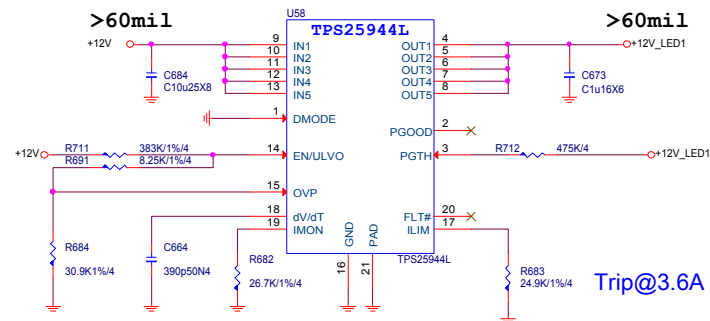
2 AUDIO/IO Cover LED



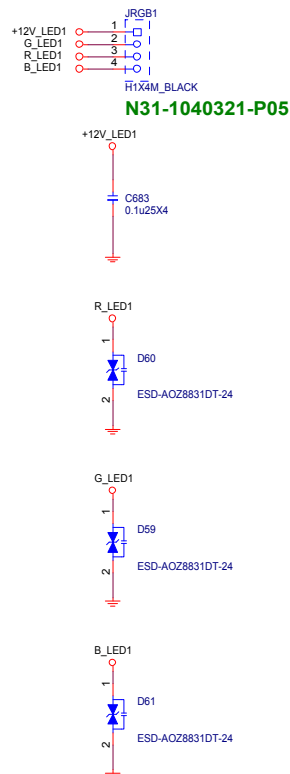
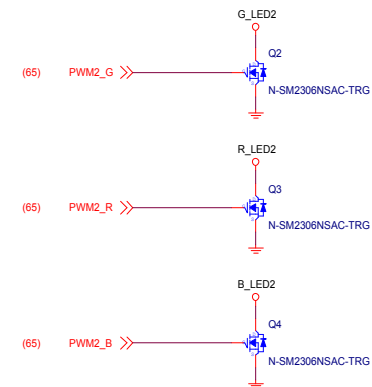
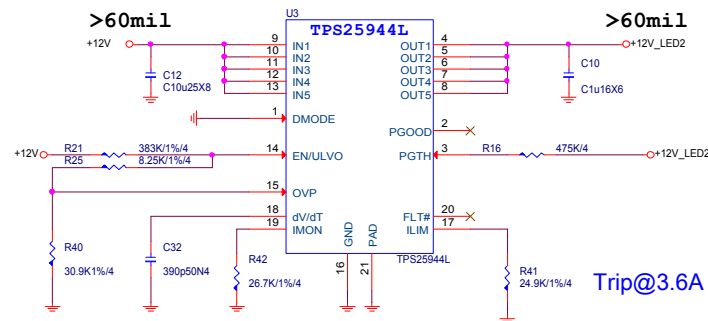
3 MOS HEATSINK LED



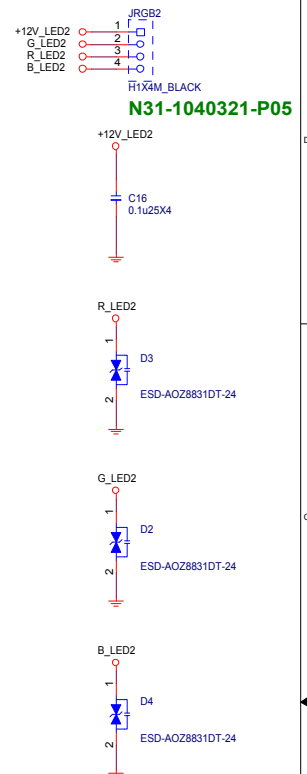
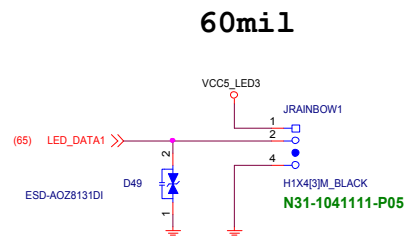
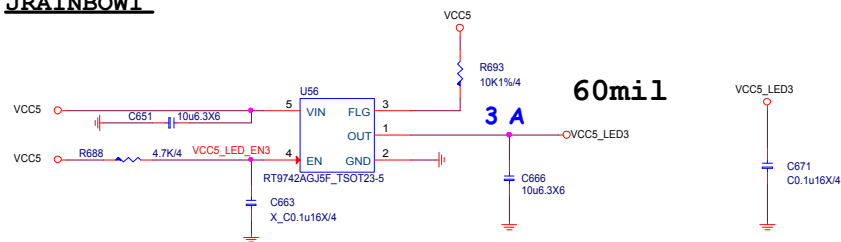
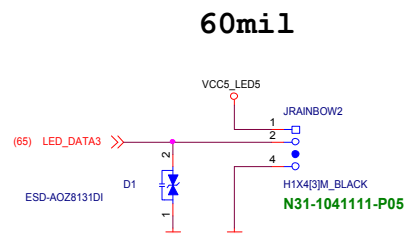
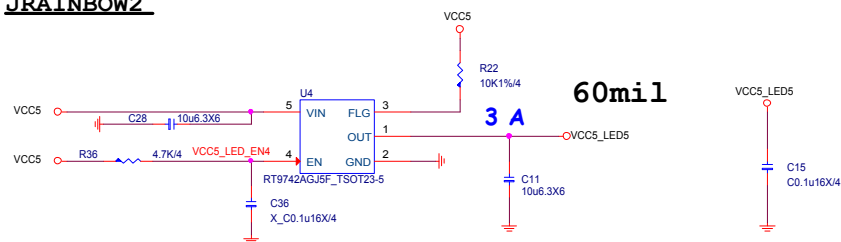
JPIPE:PIN1:output ,PIN2:input
PIN2:MCU IN
PIN1:HEATSINK OUT

JRGB1

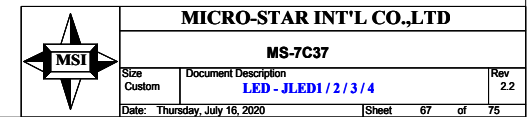
外接LED 燈條 (RGB)
 ---- PCB 文字面 (JRGB1)
 ---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRGB2

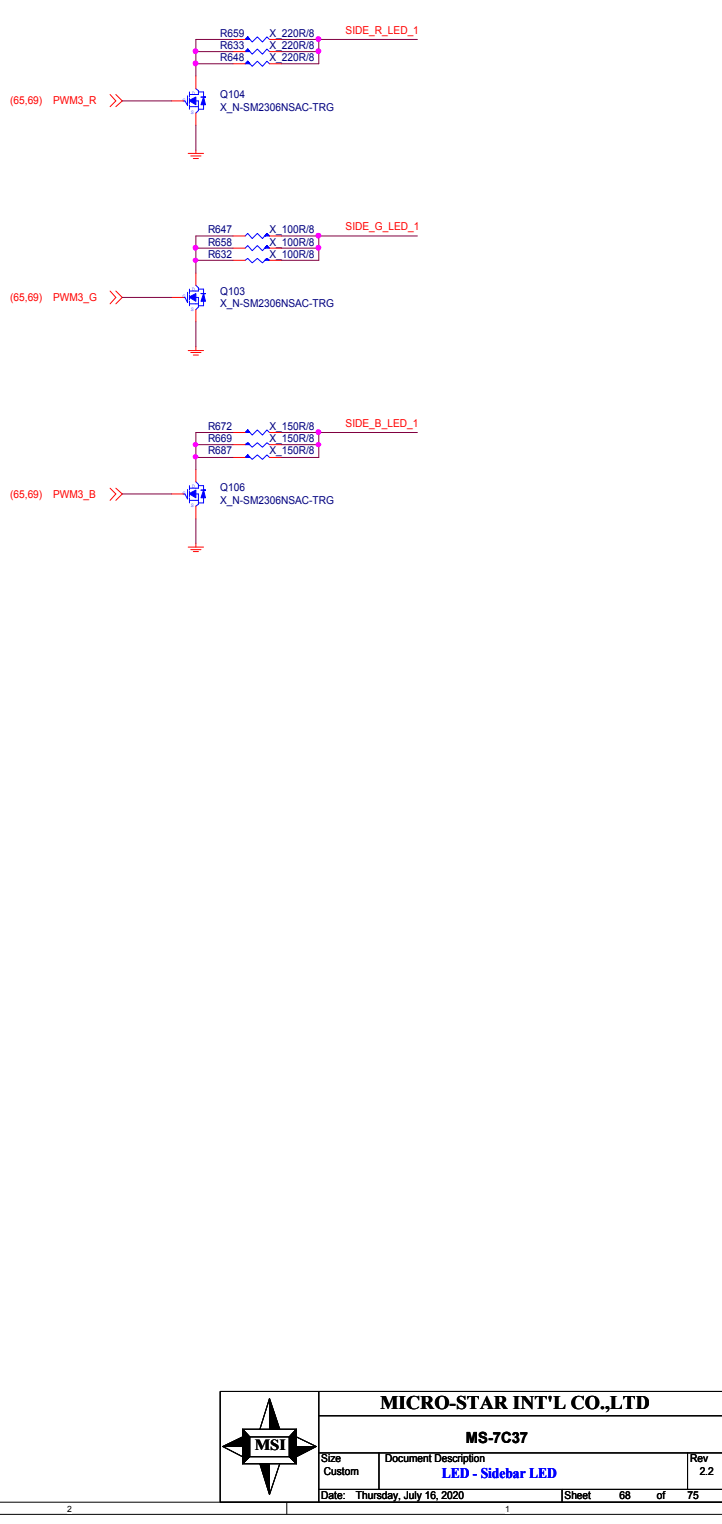
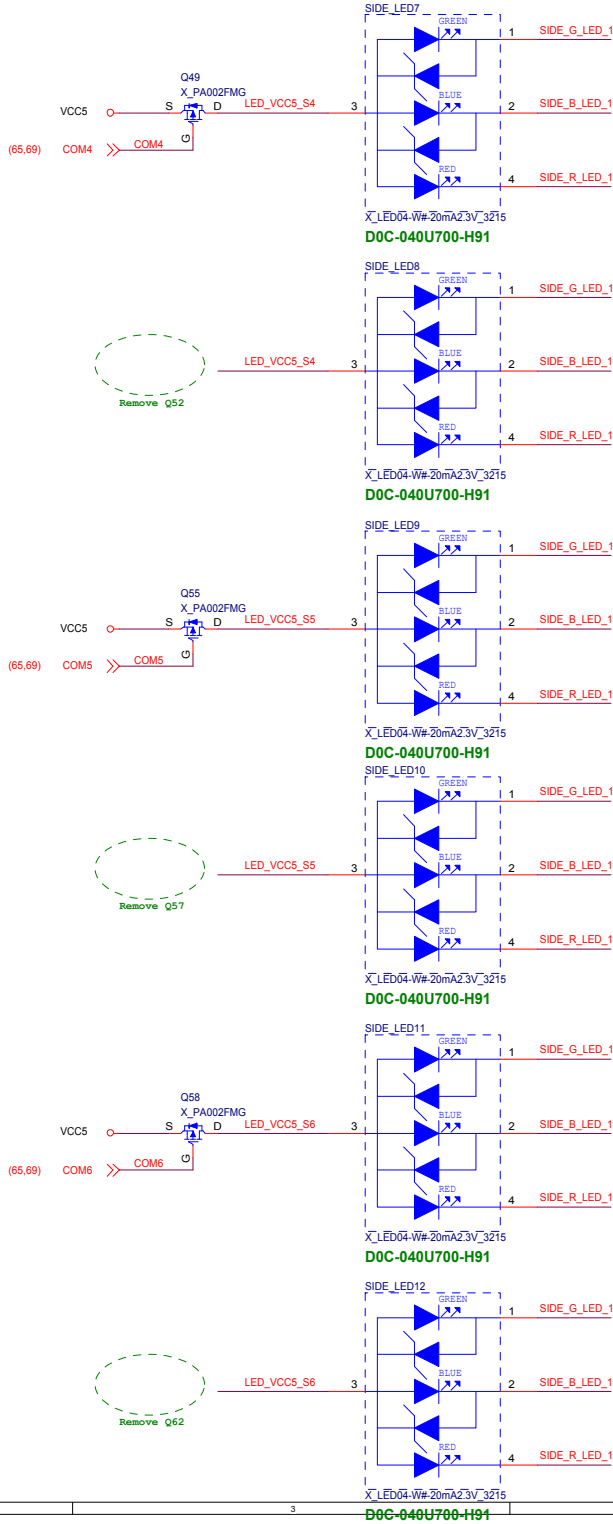
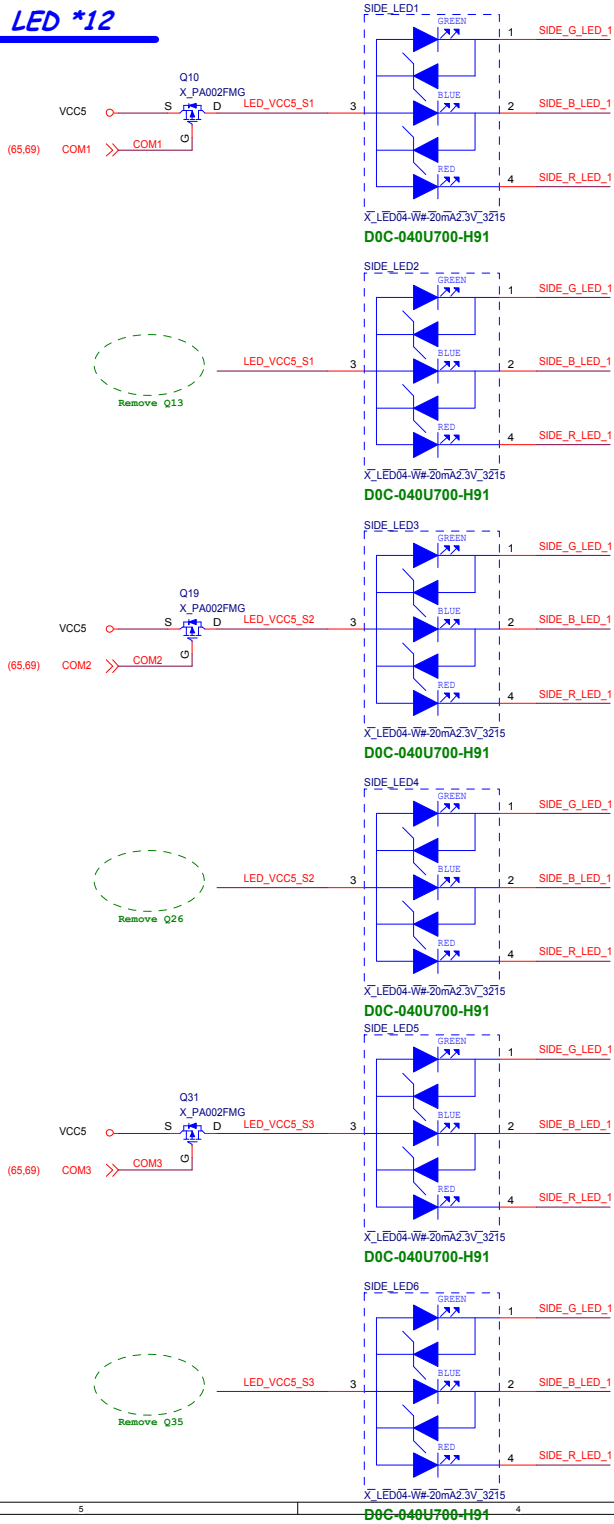
----- 外接LED 燈條 (RGB)
----- PCB 文字面 (JRGB2)
----- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRAINBOW1JRAINBOW2

JCORSAIR1



Sidebar LED *12

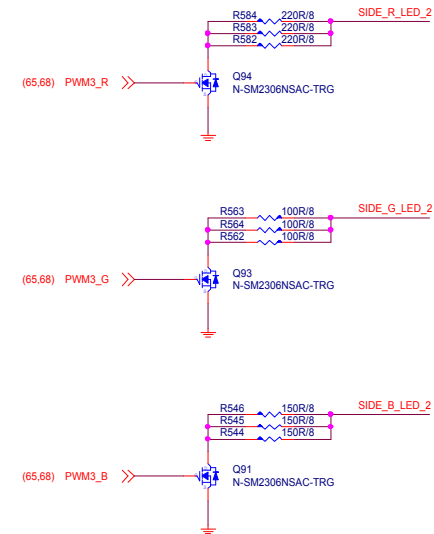
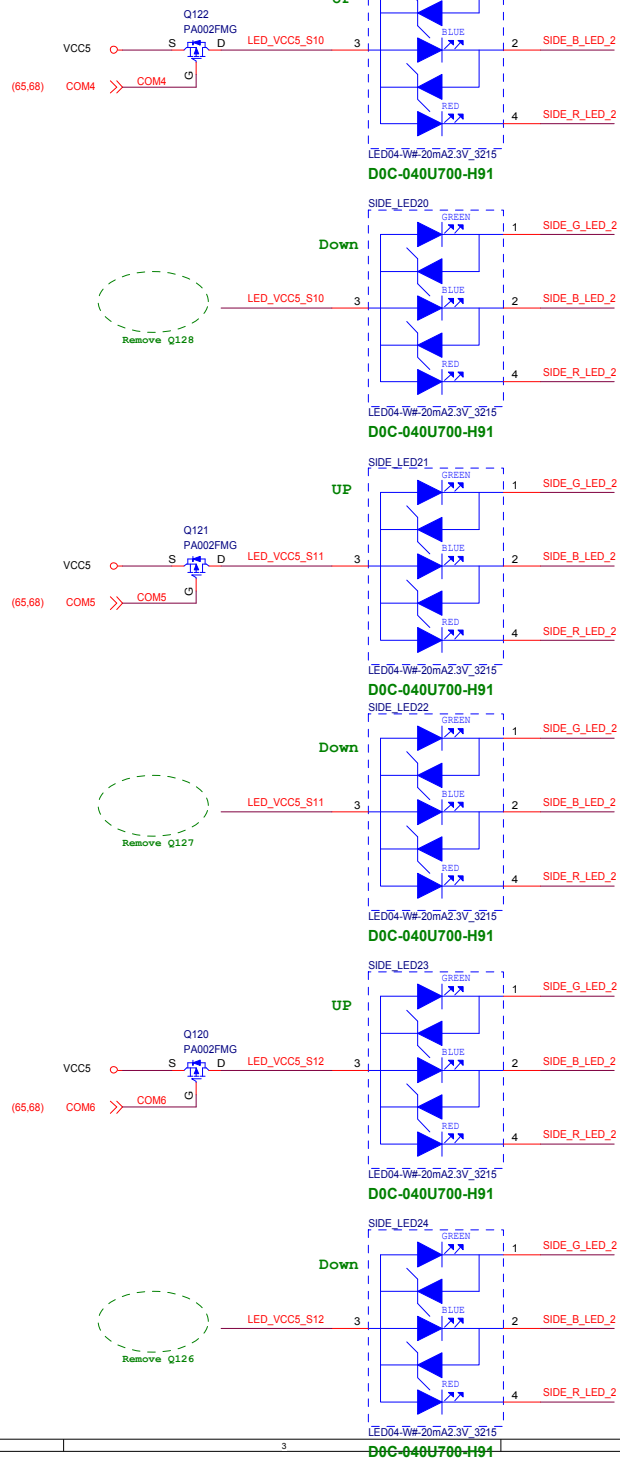
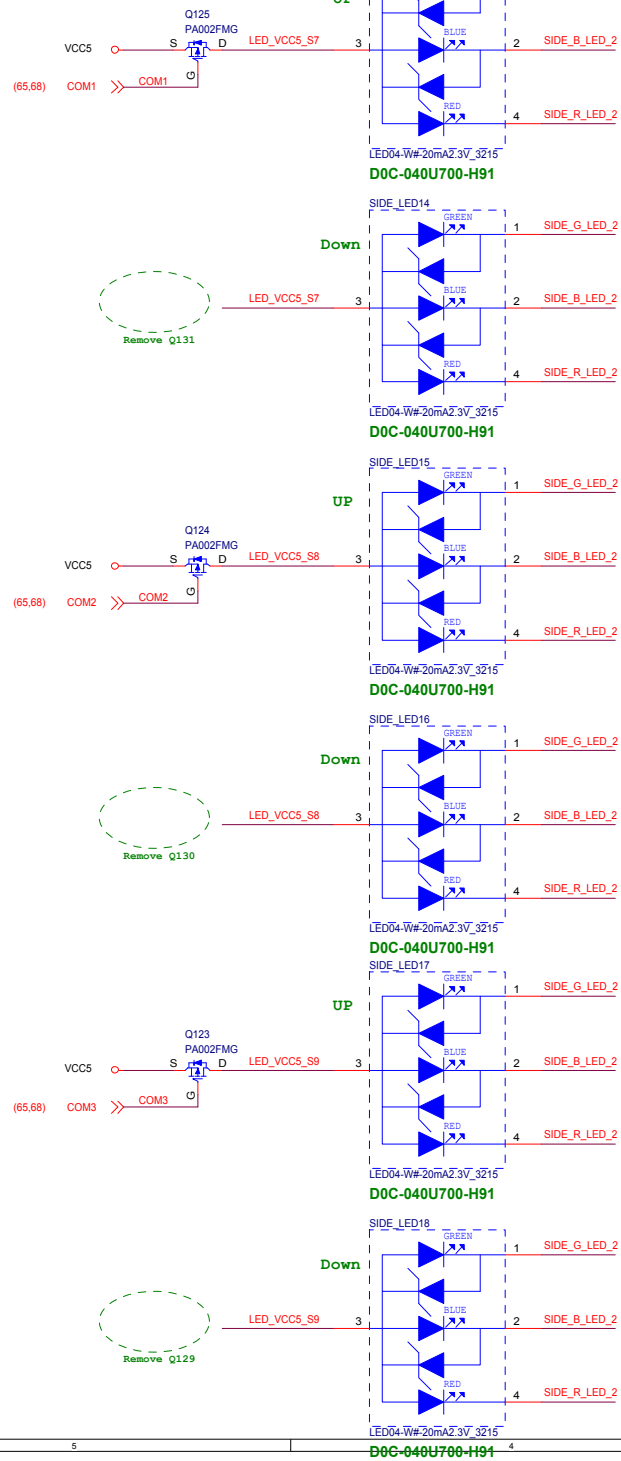


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Size Custom	Document Description LED - Sidebar LED	Rev 2.2
Date: Thursday, July 16, 2020	Sheet 68 of 75	

Market Name LED *12

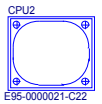


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	LED - Market Name	2.2
Date: Thursday, July 16, 2020	Sheet 69 of 75	

CPU Socket



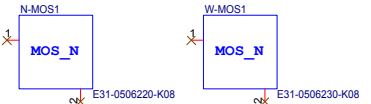
E95-0000022-C22

PCB



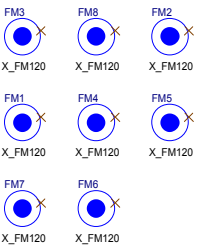
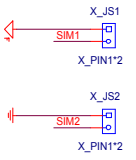
PD0-07C3722-E48

MOS HEATSINK

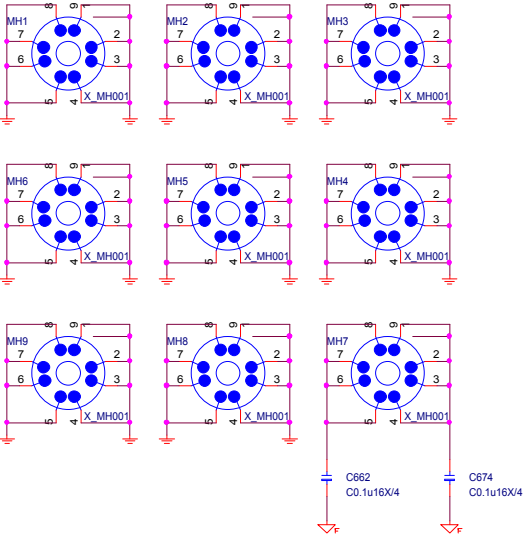


IO COVER

Simulation



Optics Orientation Holes



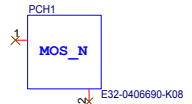
MANUAL PART

UEFI1
G51-M1SPXXA-A09
G51-M1SPXXA-A09
HDMI_LA1
Label
HDMI
HDMI LABEL
Y01-RHDMI03-000

NAHIMIC1
X_Y02-MU00100-NAH
Y02-MU00100-NAH

XSPILT1
X_Y02-MA00401-XSP
Y02-MA00401-XSP
SSE1
X_Y02-MA00101-SSE
Y02-MA00101-SSE

PCH HEATSINK



Audio COVER



DDR COVER